Development of a Cu Alloy Sputtering Target

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We have developed Cu alloy films with good adhesion to glass and resin substrates. For flat panel display (FPD) applications, particularly wiring material of the next generation high definition TV, high thermal resistance is required. Compared with the Cu/Ti and Cu/Mo films commonly used as thin film transistor (TFT) wiring metals, our newly developed the Cu alloy exhibits higher thermal resistance characteristics. In addition, for printed circuit board (PCB) applications, the new Cu alloy film contributes to cost reduction by simplifying the etching process compared with Cu/Ti film as the general wiring material.

1. Introduction

In recent years, the development trends in FPD applications for displays used in TVs have been towards increased screen size and enhanced resolution beyond the HDTV level[1)]. Today, 4K panels (3840 × 2160) with quadruple the number of pixels as in Full HD (1920 × 1080) are becoming mainstream. In the future, we expect to see support for 8K panels (7680 × 4320) with 16 times the number of pixels. An 8K panel will constitute the ultimate two-dimensional projection system, enabling viewers to experience unprecedented realism, as well as the feeling of being actually present or immersed[2)].

Meanwhile, in the field of electronic device mounting, as mobile information terminals such as smartphones and tablet PCs have rapidly become widespread in recent years, remarkable advances in their miniaturization and functional enhancement have occurred. As a result, demand is increasing for technologies for mounting semiconductor chips at higher densities. In response, the need is increasing for making the printed circuit boards (PCB) onto which these chips are mounted denser and thinner[3)].

A type of Cu film commonly employed for low-resistance wiring material is used in a stacked structure that includes for the adhesion layer a high-melting-point metal such as Ti or Mo. This is necessary because pure Cu does not adhere well to glass and resin substrates. However, Ti poses a problem because Cu/Ti stacked film cannot be easily wet-etched in a batch, while the problem with Mo is that galvanic corrosion causes etching failures in Cu/Mo stacked film. In both cases, the problem must be corrected using post-processing etching, which results in increased costs.

As we have already reported, excellent adhesion and barrier characteristics can be obtained by forming a Cu alloy oxide film on the interface with the substrate using sputtering with oxygen mixed in[4)]. A Cu wiring process using a Cu-Mg-Al target results in excellent adhesion to glass substrates[5)]. In preparation for 4K and 8K panels, it will become necessary in FPD applications to make the Cu layer thicker in order to reduce the resistance of the wiring. As the film deposition time increases in order to make the Cu film thicker, there is concern about raising the substrate temperature. Therefore, we recently evaluated the Cu-Mg-Al alloy process in order to achieve low-resistance wiring for 4K and 8K panels.

Meanwhile, high-density mounting applications require Cu alloy films capable of adhering strongly to the glass epoxy resin substrate. Furthermore, in terms of wet etching characteristics, if the alloy is soluble in a Cu-based chemical solution, the seed layer can be batch-etched, reducing the number of process steps, which can be expected to reduce costs. After evaluating various materials, we have developed a Cu-Al-X alloy that exhibits excellent adhesion to resin and can also be dissolved in a Cu-based wet etching solution.

2. Characteristics required of TFT wiring for use in high-definition TVs

It can be seen in Figure 1 that the gate width in a conventional full HD panel is approximately 40 μm. However, in a high-definition 4K panel, the gate width narrows significantly to approximately 10–20 μm, requiring a device design in which the TFT wiring width becomes ultra narrow. Microsizing the wiring increases the wiring's resistance, which can result in signal delay. This problem can be addressed by switching to a low-resistance material or by making the wiring film thinner. Gate wiring films for use in high-definition TVs must exhibit the following characteristics:

- ■ Low resistance
- ■ Adhesion to glass substrates and oxide layers
- ■ High thermal resistance
  - Against rising temperatures during deposition of the substrate that could result from thickening of the Cu layer
  - Against thermal loads in post-processing
- ■ Others
  - Wet etching characteristics
  - Electrical contact characteristics with ITO
  - Surface flatness (hillock resistance)

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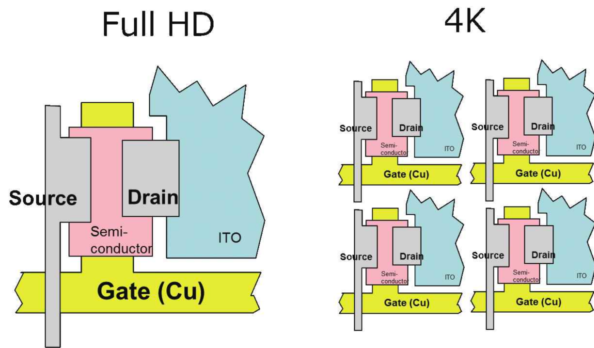

Figure 1 Planar image of TFT wiring of Full HD and 4K.

2.1 Low resistance

As display size has increased, Cu wiring (with specific resistance of 2 μΩcm), which has a lower resistance than Al-based wiring (with specific resistance of 3–5 μΩcm), has replaced the latter, becoming the mainstream in TFT wiring. A Ti-Mo-Mo alloy is generally used for the adhesion layer of Cu wiring, resulting in a stacked structure consisting of a pure Cu layer, an adhesion layer, and the glass. In the case of high-definition TVs, the film thickness of the Cu layer is doubled to reduce the resistance.

2.2 Adhesion to glass substrates and oxide layers

The Cu-Mg-Al alloy possesses excellent adhesion to glass substrates and oxygen-containing substrates made of oxide layers. Figure 2 shows a TEM-EDX image of a cross section of an as-deposited film on Cu/Cu-Mg-Al/Glass. Figure 3 shows the EDX profile of the same sample. These images show precipitation of Mg and Al in the interface between the Cu-Mg-Al alloy film and the glass. This is presumed to be the result of the additives to the alloy, such as Mg and Al, having precipitated in the film boundary and reacted with the oxygen in the substrate, thus forming an oxide layer. We have concluded that because an oxygen-containing substrate, such as a glass substrate, is a substance made up of covalent bonds, bonding affinity improved the adhesion characteristics.

2.3 Thermal resistance

As the Cu film thickness is increased to reduce the resistance of the wiring, the thermal load increases as a result. In film deposition using sputtering, the substrate is subjected to a thermal load from radiant heat and latent heat, and therefore thermal resistance during the Cu film deposition process is required.

More recently, because of the trend towards large-screen, high-definition displays, efforts are underway to develop high-mobility semiconductors, and other such devices, as a backplane technology. For oxide semiconductors, which have been attracting attention in recent years, high-temperature annealing is a necessary technology for achieving high mobility and stability[6]. Meanwhile, for Si-base semiconductors, a localized laser annealing technology is being developed with the goal of achieving partial crystallization[7].

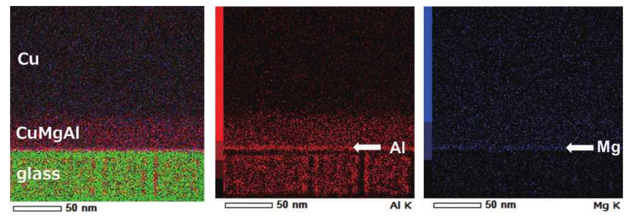

Figure 2 Cross section TEM-EDX of Cu/Cu-Mg-Al/glass.

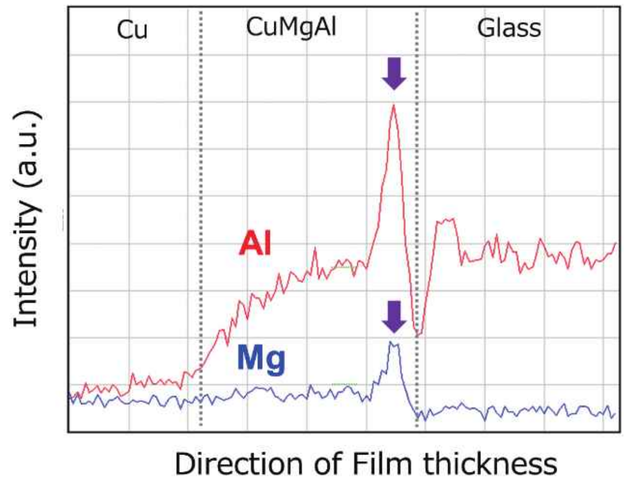

Figure 3 EDX Profile of Cu/Cu-Mg-Al/glass.

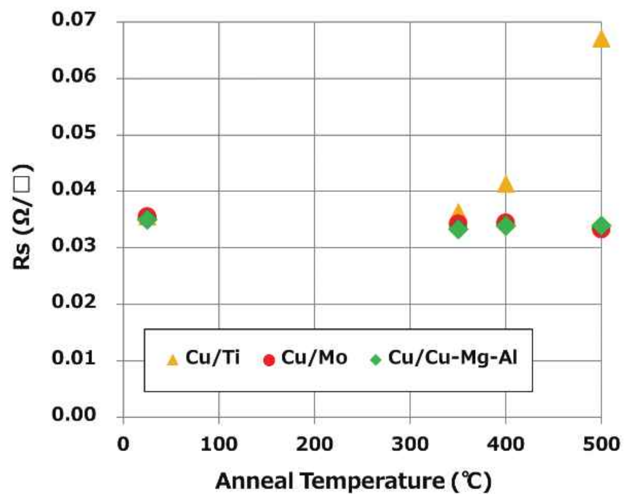

Figure 4 Sheet resistance after vacuum annealing (Cu/Ti, Cu/Mo, Cu/Cu-Mg-Al).

Higher thermal resistance will become necessary during the processing that follows the formation of TFT wiring using the next-generation technology.

To evaluate thermal resistance, we compared resistance behaviors and surface shapes before and after vacuum annealing for a Cu/Cu-Mg-Al stacked film, a Cu-Ti stacked film, and a Cu/Mo stacked film. Figure 4 shows the resistance result of each type of stacked film after vacuum annealing (at 1 Pa and 350–500°C, for 30 minutes). In the Cu/Ti stacked film, resistance increased at 400°C or higher compared to the as-deposited film, while in the Cu/Mo and Cu/Cu-Mg-Al stacked films, resistance did not deteriorate

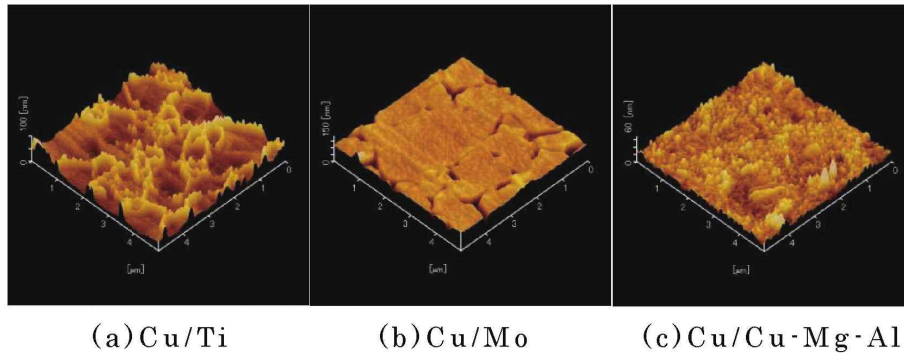

Figure 5 AFM Image after 500°C anneal (Cu/Ti, Cu/Mo, Cu/Cu-Mg-Al).

Table 1 Ra and P-V of AFM Data.

AFM Data	Film Structure (on Glass)	as depo.	350℃ anneal	500℃ anneal
Ra	Cu/Ti	2.2	2.2	13.9
	Cu/Mo	2.3	3.5	5.3
	Cu/Cu-Mg-Al	2.3	3.3	4.3
P-V	Cu/Ti	25.1	30.9	98
	Cu/Mo	24.9	75.0	184
	Cu/Cu-Mg-Al	25.0	53.2	65

even after annealing at 500°C. We concluded that Ti diffused into the Cu film because Cu and Ti are materials that form intermetallic compounds under thermal load[8].

Figure 5 shows the AFM images after vacuum annealing of the various stacked films (at 500°C). Table 1 shows the Ra and P-V values of the as-deposited film and the film after vacuum annealing (at 350°C and 500°C). In the Cu/Ti stacked film, the surface roughness in the post-annealing AFM image and the increase in the Ra value confirm the effect of Ti diffusion into Cu. No mutual diffusion was recognized in the Cu/Mo stacked film inasmuch as resistance did not deteriorate. However, a crack was confirmed based on the AFM image and an increase in the P-V value. It is presumed that this occurred because the difference in the thermal expansion coefficients between Cu and Mo is greater than between Cu and Ti or Cu-Mg-Al. The effect of annealing on the surface shape of the Cu-Mg-Al stacked film is smaller than that on Ti or Mo, implying that this stacked film has superior thermal resistance at high temperatures.

3. Characteristics required of seed layers to be used in high-density mounting

Electroless plating has traditionally been used for Cu seeding on PCBs. However, to accommodate the trend toward higher density, it has become essential to use sputtering to deposit a Cu/Ti film for the seed layer and to use electroplating for Cu embedding. With the electroless plating method, a chemical is used prior to plating to roughen the surface of the substrate resin, and an anchoring effect is used to ensure adhesion. However, in high-density, ultra-fine wiring, there are concerns that a high degree of surface roughness might result in stripping the wiring, loss of signal transmission, and plating defects inside due to holes. Meanwhile, in the case of the sputtering method, by depositing a metallic film (normally Ti), which acts as the adhesion layer between the resin substrate and the seed Cu film, excellent adhesion is achieved even on resin substrates with a low degree of surface roughness[9), 10)].

High-density mounting of IC chips requires an interposer (package substrate), which is a relay substrate for connecting the chips to the wiring. Figure 6 shows the structure

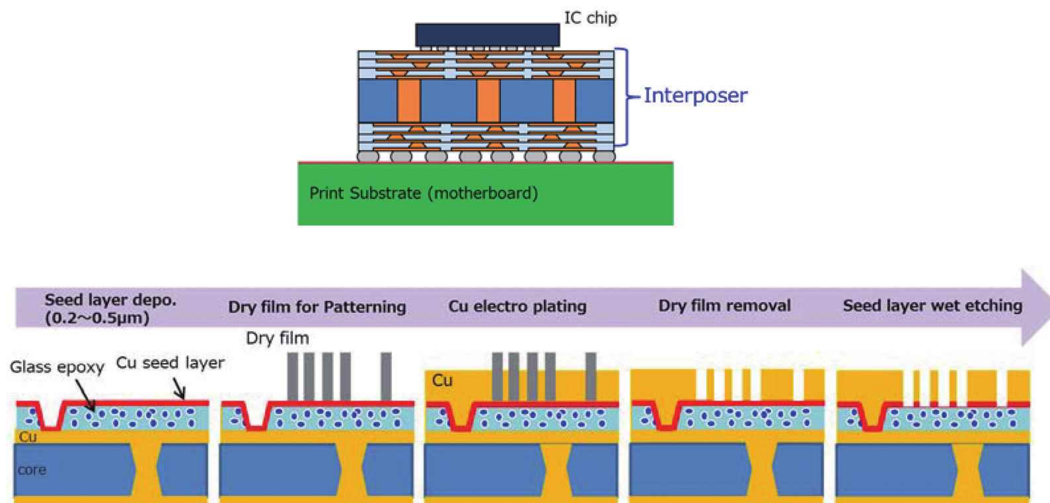

Figure 6 Semi-Additive Process Flow for PCB Interposer.

of and manufacturing process for an interposer. The interposer is manufactured by alternately stacking four to six layers of a resin material (build-up material), which is an insulation layer for wiring, and Cu wiring on each surface of the core substrate (glass epoxy substrate with copper foil). This is called a semi-additive process (SAP). In this process, the wiring is formed in the following sequence: seed film deposition (sputtering), wire patterning using photoresist, Cu electroplating, resist removal, and etching away of the seed layer in unneeded areas. The following characteristics required of seed layers and adhesion layers to be used in high-density mounting are described below:

- ■ Adhesion to the glass epoxy resin substrate
- ■ Wet etching characteristics

3.1 Adhesion to the glass epoxy resin substrate

A glass epoxy resin is a material made by impregnating glass filler with an epoxy resin. It possesses excellent characteristics in terms of insulation, non-flammability, dimensional stability, and material strength. The glass epoxy resin film evaluated and utilized by the authors was an Ajinomoto Build-up Film. We selected Al and element X as additive elements to the Cu alloy, with the goal of improving adhesion to glass and resin. The evaluation procedure is described below.

Preheating of the substrate (130°C, 30 minutes)
→ Ion gun treatment (thermal oxide film equivalent: 3-nm etching)
→ Sputtering (Cu/Ti and Cu/Cu-Al-X alloys)
→ Cu electroplating (30 µm)
→ Post-annealing (180°C, 30 minutes, 1 hour in air) → Peel strength measurement (1)
→ Post-HAST (130°C, 85%, 100 hours) → Peel strength measurement (2)

We carried out post-annealing, assuming post-processing, as well as a HAST (Highly Accelerated Stress Test). Figure 7 shows that the Cu/Cu-Al-X alloy demonstrated a high level of peel strength that was equal to or greater than that of Cu/Ti, even after annealing at 180°C and HAST.

3.2 Wet etching characteristics

In the case of the Cu/Ti process, two etching solutions were used for Cu and Ti. For etching Ti, a solution consisting of H_2O_2 and an alkali-free chemical is normally used. However, this type of solution has the drawback of poor solution stability, which may pose a concern about higher production cost due to short solution life and the high frequency of waste liquid disposal. Therefore, in order to extend the life of the etching solution, development of chemicals with improved stability is also underway[11].

In contrast, in the case of a Cu/Cu alloy process, because only a single etching solution for Cu is needed, elimination of a processing step and reduction in production costs can be expected. However, in wet etching using the SAP, the unneeded seed layer is removed while the Cu plating is exposed, as described above, making it possible to determine an etching selectivity ratio between the seed layer and the Cu.

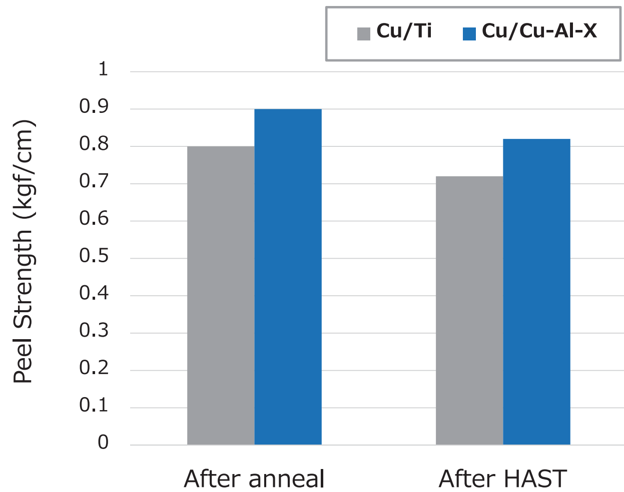

Figure 7 Peel strength of Cu/Ti and Cu/Cu-Al-X.

Table 2 Wet Etching Rate of Cu-Al-X and E-plated Cu.

Etchant	Cu-Al-X E.R. (µm/min.)	E-Plated Cu E.R. (µm/min.)	Cu-Al-X/E-Plated Selectivity
H_2O_2 series	0.72	0.50	1.4

In our study, we used an H_2O_2-based chemical as the etching solution, and we compared the etching rates of a single Cu-Al-X alloy film and an E-plated Cu film. As shown in Table 2, a higher etching rate was obtained with the Cu-Al-X alloy than with the E-plated Cu film. These results make the Cu-Al-X alloy promising for use in an SAP that will employ it both as the seed layer and the adhesion layer.

4. Conclusion

We have developed a new Cu alloy sputtering target for use in the wiring of high-definition TVs and for mounting electronic parts at high density. In high-definition TV applications, the newly developed alloy can be expected to be used in a wiring process possessing high thermal resistance and low electrical resistance, which will also be able to support future technical innovations in devices. Additionally, in high-density mounting applications, the newly developed alloy will be able to contribute as a cost-reducing wiring process as the number of application devices expands in the future.

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