High-density Panel Level Package Solution

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High-density packaging technologies such as 3D, 2.5/2.1D scheme basing on PCB (Print Circuit Board) substrate are among key technologies to satisfy the requirements from the both smart semiconductor devices and smart functional devices. ULVAC has been continuously developing manufacturing solutions for high-density packaging. In this paper, build-up multilayer technology solutions consisting of etching, ashing and PVD (Physical Vapor Deposition) sputtering to make the high density interconnection PCB panel substrate, will be introduced.

1. Introduction

In recent years, because of the rapid spread of mobile terminals typified by smartphones and tablets, IC chips are becoming increasingly thinner and smaller. Accordingly, there is a growing need for denser and thinner IC package substrates and the core layer, which supports a substrate, is becoming thinner and thinner[1)]. On the other hand, larger chips, and accordingly larger substrates, are required for high-end servers, etc. To keep up with the trends and meet the needs for higher-density packaging in a wide range of fields from mobile applications to server applications, the use of semiconductor miniaturization technology for build-up wiring formation for PCB (Printed Circuit Board) substrates has been studied. PCB substrates are square substrate (panels) with a side length of 510 mm or more, and in addition to understanding warpage, heat resistance, and their mechanical characteristics, there are unique challenges to tackle in handling various panels, challenges that are different from those in conventional silicon wafer processes[2)]. This paper introduces the latest on ULVAC's panel-level package solution, a technology released for the first time in the world.

2. Dry panel-level build-up process

2.1 Application of dry desmear with plasma etching technology

Figure 1 shows the PCB interposer production (build-up) process. A CO_2 laser drill is used to form a via connecting the upper and lower insulating film layers. After via formation, residue called "smear" remains at the bottom of the via. The build-up film is made of a mixture consisting of epoxy resin and SiO_2 particles called "silica filler" and this mixture is generally called a "glass epoxy film." Smear consists of epoxy resin and silica filler as well. Proceeding to the next process without removing smear results in low wiring reliability, such as low adhesion of Cu and increased wiring resistance. Therefore, the desmear process is essential. With the current generation, smear can be removed in a wet environment, but various new challenges are arising because vias are becoming smaller and smaller (50 μm or less). These challenges include, for example: (1) difficulty in applying the same wet processing conditions to different film qualities or adjusting these conditions; (2) limitations on controlling the dimensional conversion accuracy of micro vias (swelling problem); (3) limitations on the smoothness control of via

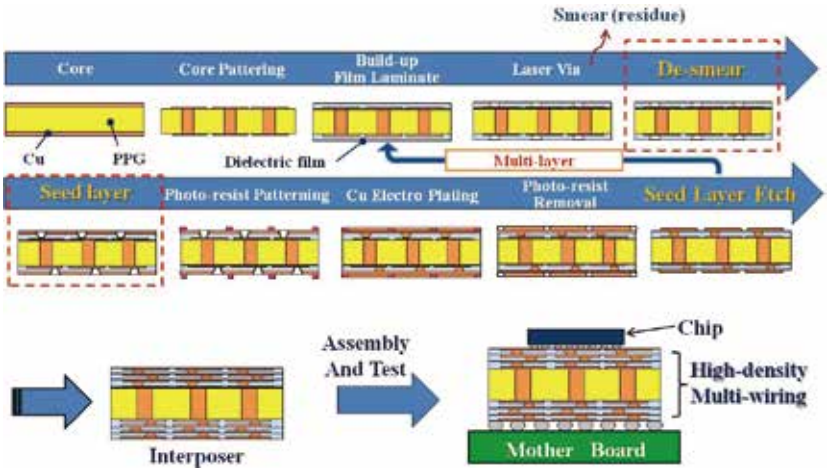


Figure 1 Semi Additive Process Flow for PCB Interposer.

sidewalls; and (4) weakness of corresponding to high aspect ratios (>2). Figure 2 demonstrates the need to shift from wet desmear to dry desmear[3]. As can be seen in the figure, with dry etching, smear can be removed and at the same time, the irregularities on the silica filler on the via sidewall can be smoothed out. For this paper, A CCP-RIE (Capacitive Coupling Plasma-Reactive Ion Etch) etching system was used and ABF (Ajinomoto Build-up Film) was mainly used as the glass epoxy film.

Figure 3 shows the etching rates of the glass epoxy films whose surfaces were etched with SF6, CF4, and O2 gases. The etching rate is highest when SF6 is used and lowest when O2 is used. This is because the silica filler cannot be etched with O2 only. Figure 4 shows the trends in the roughness of the glass epoxy surfaces etched with different mixing rates of these gases. From this figure, it can be seen that the smoothness of the etched surface can be controlled by using the gas mixing rate that provides nearly the same etching rate for the epoxy resin and silica filler. The surface with wet desmear is provided for comparison, which clearly shows that the surface with wet processing is rougher. These results can be considered to demonstrate one advantage of plasma etching, namely, that it is more suited to optimizing (adjusting) individual plasma conditions (gas mixing rate and other parameters) for each material and type than the wet process.

Figure 5 shows the SEM (Scanning Electron Microscope) image taken after a via of 50 μm in diameter was formed on an ABF film (film thickness: 25 um) with a laser drill, the result of the EDX (Energy Dispersive X-ray Spectrometry) observation focused on the bottom of the via, and the SEM image and EDX observation result after dry desmear with plasma etching technology. The EDX result shows that carbon (C), oxygen (O), and silicon (Si) peaks were observed at the bottom of the via formed with a laser drill. These substances form smear. After dry desmear, the peak intensities of carbon, oxygen, and silicon drop significantly, indicating that the smear has been removed. The SEM image shows that after desmearing, the previously surface-roughening-treated Cu electrode is exposed at the via bottom.

Figure 6 shows enlarged SEM images of the cross section and sidewall of the via before and after dry desmear. Before dry desmear, smear is observed at the via bottom. On the via sidewall, SiO_2 filler irregularities are noticeable. After dry desmear, however, the smear has been removed and SiO_2 filler irregularities are etched by desmearing, providing a smooth sidewall. Figure 7 shows the results of deposition of seed Cu by PVD (Physical Va-

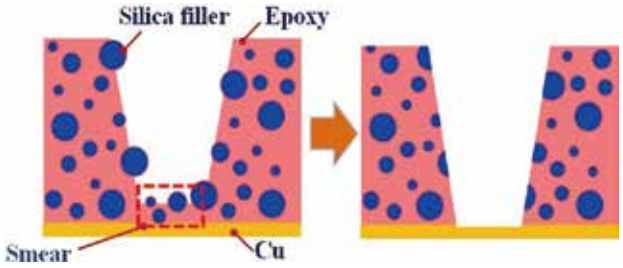


Figure 2 Dry desmear.

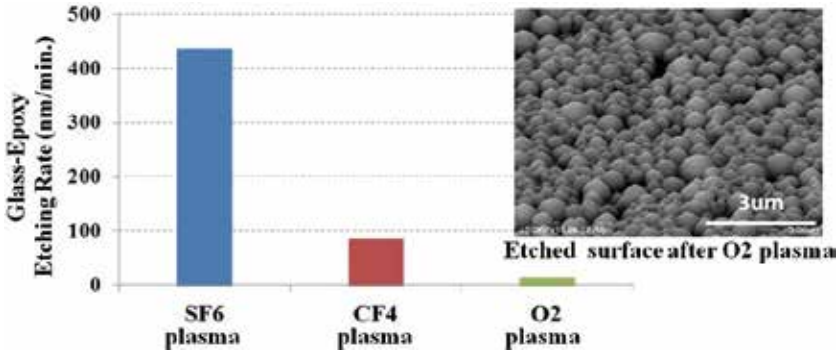


Figure 3 Glass-epoxy etch rate and etching gases.

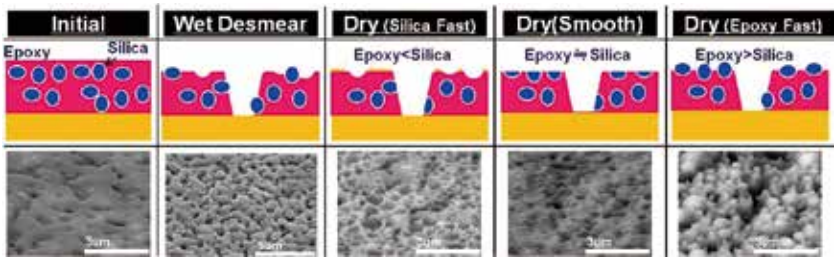


Figure 4 Etched surface of glass-epoxy after desmear.

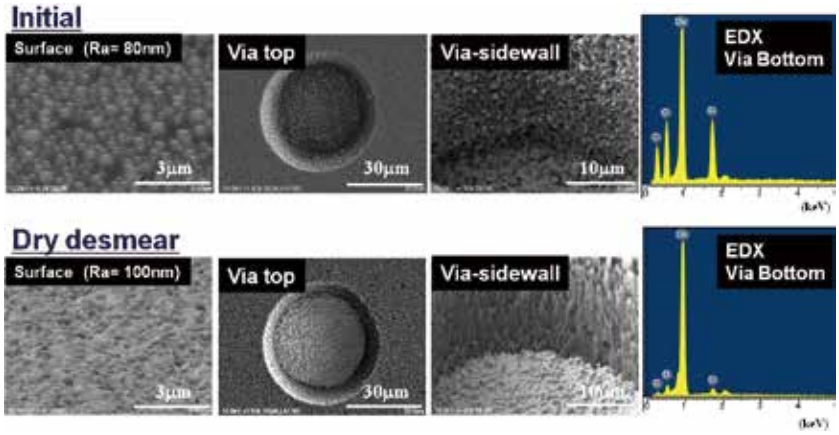


Figure 5　Dry desmear：SEM images and EDX of Via hole.

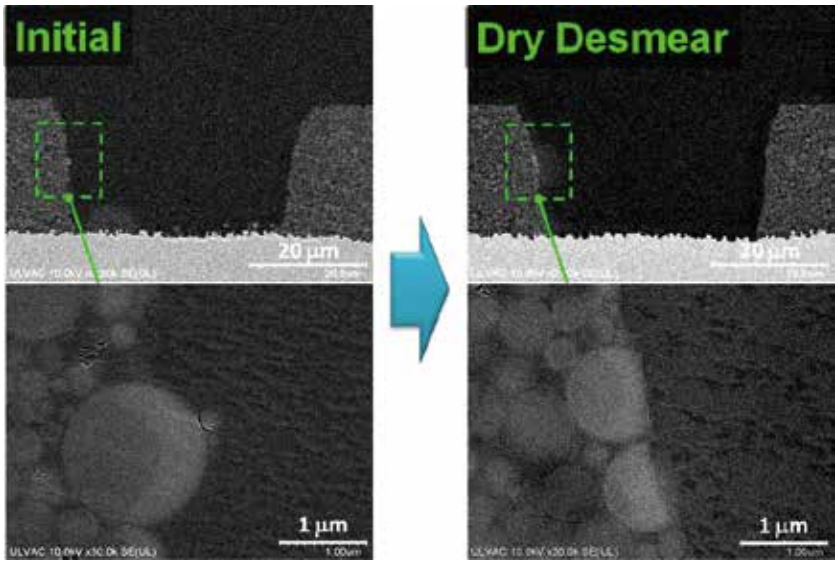


Figure 6　Via Sidewall after dry desmear.

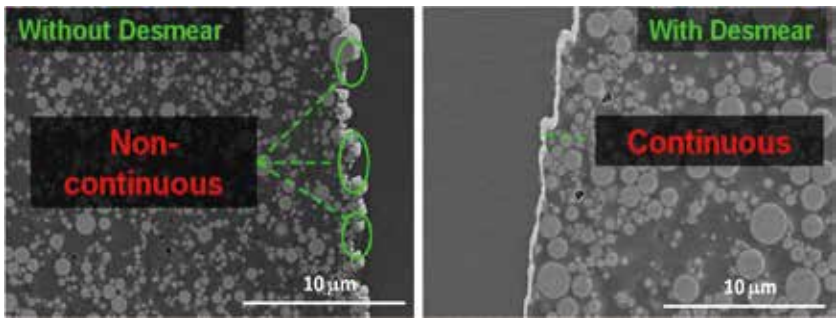


Figure 7　Relationship to seed film formation and sidewall roughness.

por Deposition) sputtering with the via before and after dry desmear. As can be clearly seen in the figure, seed Cu does not form a continuous film on the irregular sidewall before dry desmear. This result causes a risk of improper electrolytic plating in the next process. On the other hand, the seed Cu forms a continuous film after dry desmear[4]. As above, because it has been demonstrated that the dry desmear method with etching technology provides flat and smooth surfaces that cannot be obtained with conventional wet desmearing and it can be used to keep up with the miniaturization trend, the dry desmear method is considered to be an essential technology for next-generation high-density build-up wiring formation.

2.2　Application of PVD sputtering for next-generation Cu wiring formation—Sputtering system for panel substrates “SMV-500F”™—

Electroless plating has been used for seed Cu for con-

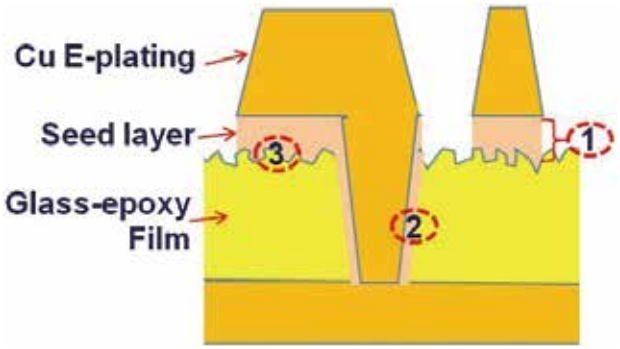


Figure 8　Technical Key Points for Sputtering Seed.

ventional PCBs. However, in order to keep up with miniaturization trends and ensure sufficient adhesion between the flat and smooth via sidewall and seed film, the Cu embedding process by seed Cu deposition with PVD sputtering and electrolytic plating are as essential as the dry desmear method mentioned in the previous section. Figure 8 shows the key points for sputtering a seed layer. The key points are (1) thin-film deposition: reduction of the seed layer thickness in the field; (2) excellent throwing power of the via sidewall: for achieving (1); and (3) high-adhesion deposition: deposition on a flat and smooth surface. As a technology for providing high-adhesion deposition on flat and smooth surfaces and depositing a uniformly thin film on a panel substrate with a side length of 510 mm or more, the PVD sputtering technology is more effective than the conventional electroless plating method.

The SMV-500F™ is a double-sided sputtering system for thin square substrates (with a side length of up to 600 mm). As shown in Figure 9, the system has three processing chambers (etching, adhesion layer metal sputtering, and Cu sputtering) and a buffer/substrate heating chamber connected to the substrate reversing/transfer chamber located at the center of the system. The substrate is degassed in the heating chamber and put into the etching chamber, where the top surface of the substrate is etched. After that, the substrate is turned over in the reversing

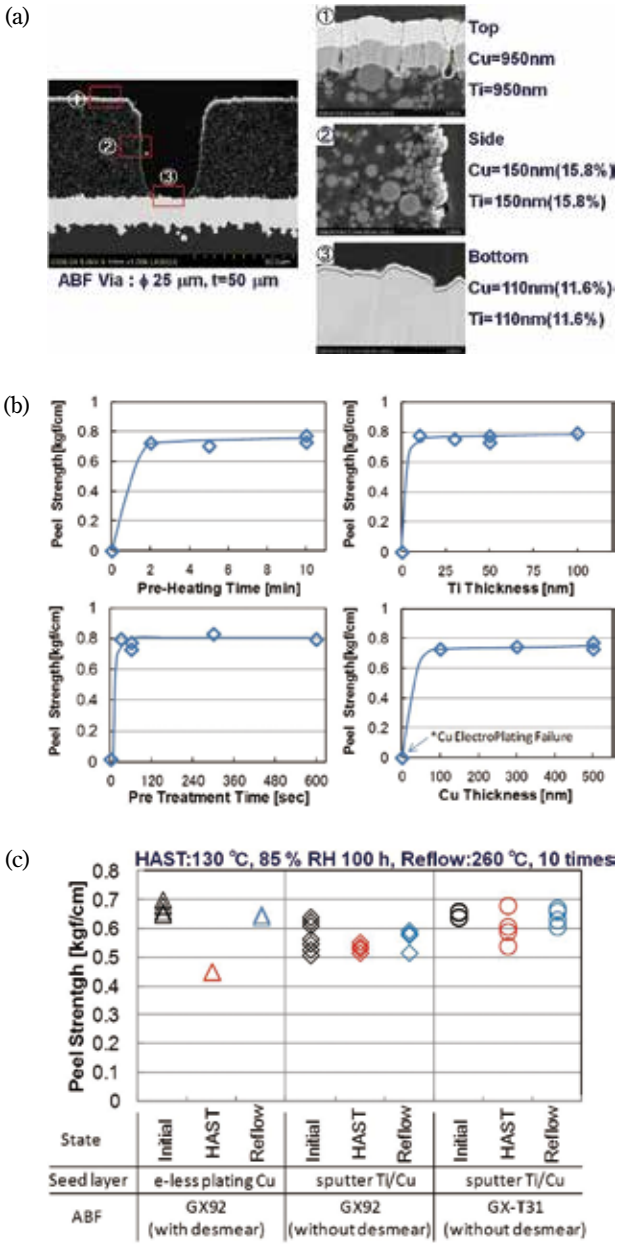


Figure 10　Deposition of seed layers by sputtering. (a) SEM, (b) Peel strength, (c) Peel strength (After hast / reflow).

chamber at the center and put into the etching chamber again, where the back surface of the substrate is etched. The substrate is put into the reversing chamber and then

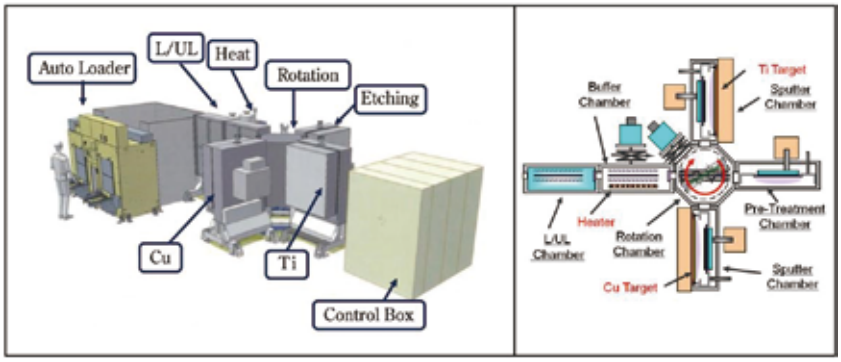


Figure 9　"SMV-500F"™.

the adhesion layer metal sputtering chamber, where the top and back surfaces of the substrate are treated in the same manner as in the etching process. Finally, the substrate is put into the Cu sputtering chamber, where the top and back surfaces of the substrate are treated. For more information, refer to the reference[5].

Figure 10 (a, b, and c) shows the results of sputtering deposition on the ABF via with this system and film evaluation, and Figure 11 shows the results of electrolytic plating after sputtering deposition[6), 7)].

2.3 Application of Ti etching with plasma ashing technology—Ashing system for panel substrates "NA-1500"™—

Build-up processes are roughly classified into single-side and double-side processes, and the requirements for the single-side process are becoming increasingly higher for application to high-density wiring interposers only with 2.1D or 2.5D resin substrates as they are known[8]. In the future, it will be required that the wiring width on the superficial layer be reduced from 20 μm to 2 μm to form fine pitch wiring on the superficial layer of a PCB substrate. Figure 12 shows an example of a process for forming wiring on the superficial layer of a PCB. This process has many similarities to the RDL (redistribution layer: re-wiring) process in WLP (Wafer Level Packaging) and requires descumming and Ti fine pattern etching. Currently, Ti is mainly etched by the conventional wet etching method, but there is a concern that there is a limit to the miniaturizing potential of this etching method and therefore, like the current WLP, the need to shift to dry etching is increasing. In general, after Ti is dry-etched, the substrate has a hydrophobic surface; therefore, a hydrophilic treatment process is required to maintain Cu plating adhesion in the next process. ULVAC's "NA-1300"™ series ashing system has proven performance in the WLP field and has also been used in many places for hydrophilic treatment. ULVAC developed new processes and a system

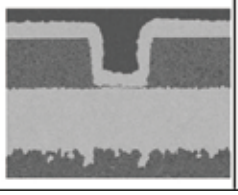
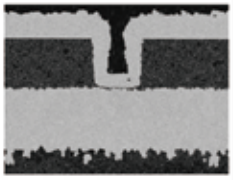
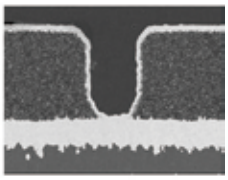
Glass-epoxy Film	ABF GX-92 t25 μm	ABF GX-92 t25 μm	ABF GX-92 t50 μm
Via Size	ϕ 35 μm A.R.: 0.7 w/o wet desmear	ϕ 30 μm A.R.: 0.83 w/o wet desmear	ϕ 25 μm A.R.: 2.0 w wet desmear
Seed Layer	Ti / Cu = 50 nm / 500 nm	Ti / Cu = 50 nm / 100 nm	Ti / Cu = 50 nm / 500 nm
Cu E-plating	15 μm	15 μm	3 μm
Cross-section Image			

Figure 11 Cu Electroplating.

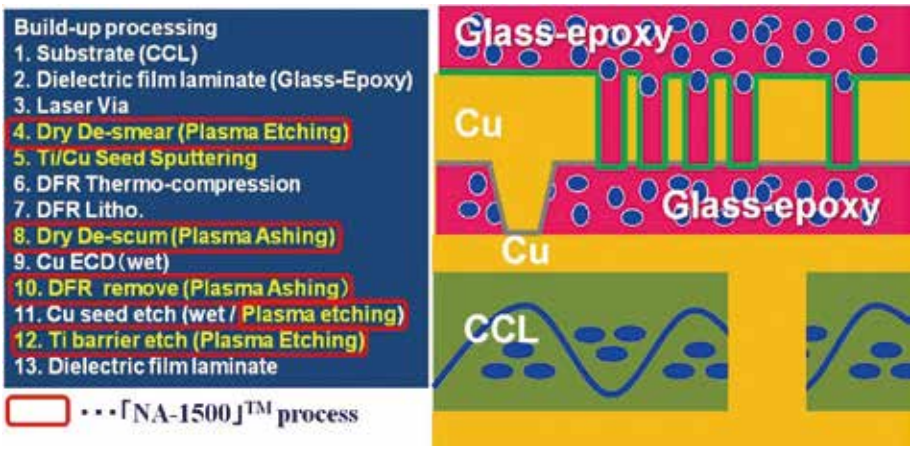


Figure 12 "NA-1500"™ Process in the Build-up PCB.

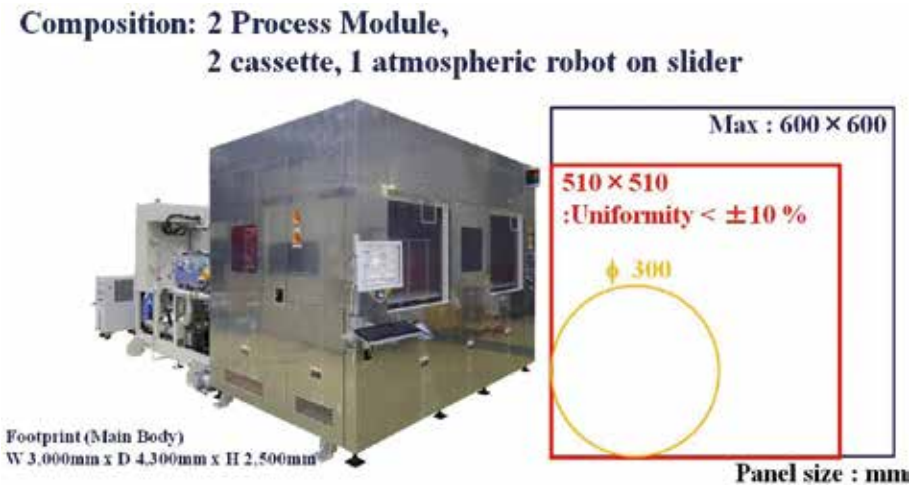


Figure 13 "NA-1500"™.

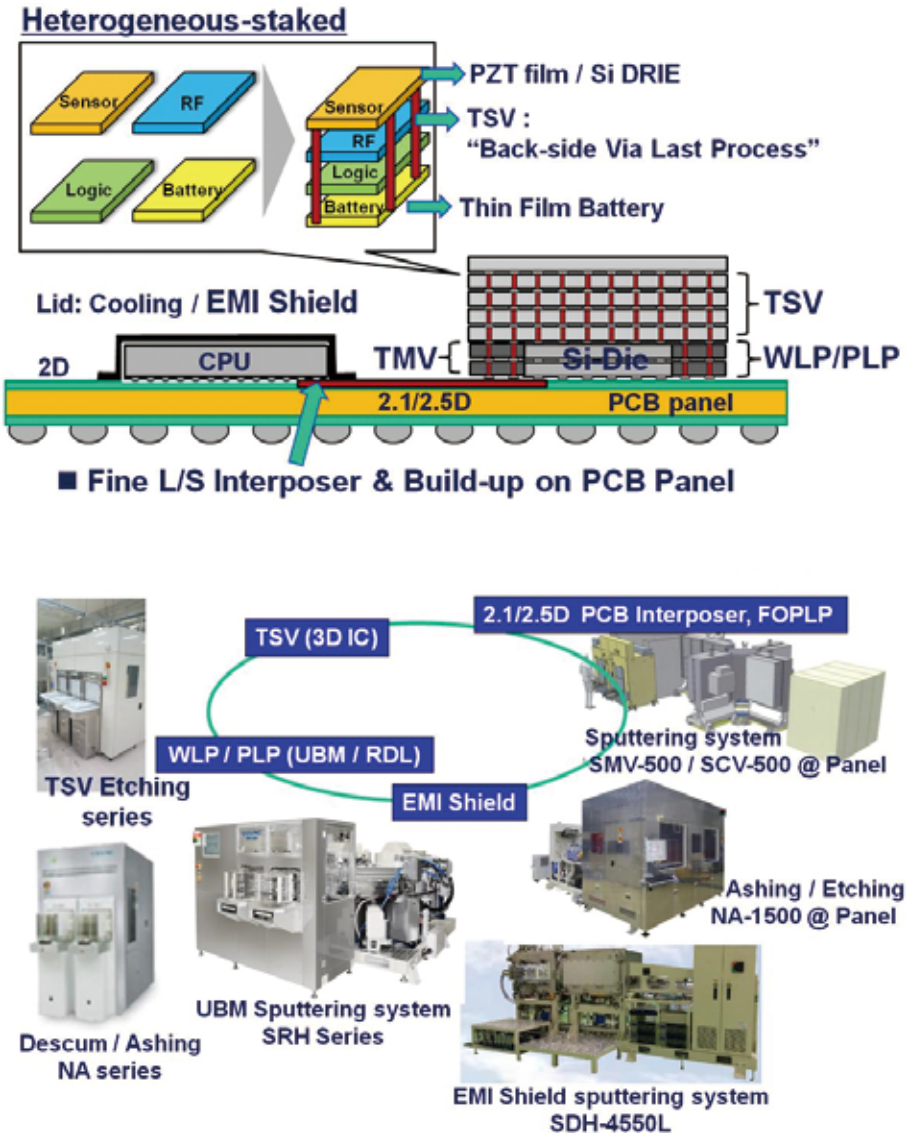


Figure 14 ULVAC High-density Packaging Technology Solutions For "Smart System".

for (1) descumming, (2) Ti etching, and (3) surface hydrophilic treatment for panel substrates and released the "NA-1500"™ (Figure 13). It uses the same plasma source as the NA-1300™. It is equipped with an RF bias, as standard, on the substrate stage side so that it can be used in many different ways for customers' next-generation de-

vice development. In addition, in CCP mode, it can perform simplified light etching and it is provided with specifications available for R&D lines based on abundant data obtained with the "NA-1300"™. When used for substrates with a side length of 510 mm or more (up to 600 mm), it provides an in-plane ashing distribution of ±10%.

3. Conclusion

This paper has introduced ULVAC's latest panel level systems and relevant process technologies aimed at adopting the dry PCB substrate build-up Cu wiring formation process to keep up with miniaturization trends. Figure 14 shows ULVAC's latest solutions for high-density packaging: "the PCB packaging solution" introduced in this paper, "the next-generation WLP/PLP packaging solution", and "the TSV packaging solution"[9]. By developing "heterogeneous packaging solutions" that combine heterogeneous chips (memory, logic, and MEMS (Micro Electro Mechanical Systems)), compound devices, TFB (Thin-Film Batteries), and other technologies, ULVAC will offer packaging solutions that are distinct from competitors' solutions and have higher expandability, thereby achieving its own "middle-end-of-line" branding strategy.

Finally, in recent years, FO (Fan-Out)-WLP is attracting much attention in the WLP field[10), 11)]. The packaging industry is aiming to produce this wafer level with panel level equipment, or reduce cost with FO-PLP. Inquiries and demonstrations are already being received from some OSAT (Outsourced Assembly and Test) manufacturers. In order to make FO-PLP a future business based on dry PCB build-up wiring business, ULVAC needs to keep an eye on this trend even at the research and development level.

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