Dielectric Material Etching Module for Electronic Device Manufacturing Lines

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We have developed a dielectric material etching module capable of processing wafers up to eight inches in diameter for electronic device manufacturing lines. This module is a narrow-gap, capacitively coupled plasma etching system powered by a 400 kHz high-frequency power supply, specifically designed for etching dielectric materials using fluorocarbon-based process gases. It offers excellent etching uniformity, reduced metal contamination, and lower particle generation, achieved through optimized components such as single-crystal silicon parts, ceramic electrostatic chucks, and an isotropic exhaust structure.

1. Introduction

The plasma dry etching equipment used in the manufacturing process for semiconductor devices can be broadly classified into two types: conductive (metal film) etching equipment that uses chlorine gases such as Cl_2 and BCl_3; and dielectric (insulating film) etching equipment using fluorocarbon-based gases such as CF_4, CHF_3 and C_4F_8. To date, various plasma sources have been developed, including inductively coupled plasma (ICP), capacitively coupled plasma (CCP), electron cyclotron resonance (ECR) plasma and surface wave plasma (SWP)[1),2)]. Currently, inductively coupled plasma etching systems are predominantly used for conductive etching processes, while capacitively coupled plasma etching systems are predominantly used for dielectric etching processes.

Capacitively coupled plasma etching systems are preferred for dielectric etching because they employ fluorocarbon-based gases. Although fluorocarbon-based gases dissociate in plasma to produce CFx, which contributes to etching, excessive dissociation releases large amounts of F radicals, which can cause problems such as decreased selectivity with respect to the resist and underlying films. Furthermore, carbon-based deposits formed in the plasma adhere to the sidewalls of the processing chamber, causing issues such as particle generation and variations in selectivity with respect to the resist. Capacitively coupled plasma etching systems are therefore preferred over inductively coupled plasma etching systems due to their narrower discharge space—which shortens the residence time of gas particles—and their ability to confine plasma between the upper and lower electrodes[3)].

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Until now, we have offered two models of magnetically enhanced inductively coupled plasma etching systems—Model NE and Model NLD—for compound semiconductors and electronic devices. Model NE features an ISM (ICP with static magnetic field) plasma source, while Model NLD features a magnetic neutral loop discharge (NLD) plasma source. However, we have not previously offered the capacitively coupled plasma etching systems mainly used in dielectric etching processes.

This manuscript introduces our development of a capacitively coupled plasma etching module specially designed for dielectric etching capable of processing 6-inch and 8-inch wafers for electronic device manufacturing lines.

2. Dielectric etching technology

A commonly used dielectric material in semiconductor devices is silicon oxide (SiO_2). As mentioned earlier, fluorocarbon-based gases are used for etching silicon oxide films in reactive ion etching (RIE). In the etching mechanism of silicon oxide using fluorocarbon-based gases, the silicon (Si) in the SiO_2 reacts with fluorine (F) to form gaseous SiFx molecules, while oxygen (O) reacts with carbon (C) to form gaseous COx molecules, allowing them to be exhausted from the chamber.

For example, CF_4, a fluorocarbon-based gas, dissociates in plasma to form CFx (x = 1 to 3) and F radicals. CFx then adheres to the surface of the silicon oxide film and forms deposits composed of carbon and fluorine. When high-energy ions accelerated in the sheath collide, the Si and O bonds are broken, causing the following reaction and advancing the etching process.

$CFx + SiO \rightarrow SiFx\uparrow + CO\uparrow$

If the ion energy is low, the deposits of accumulate on the wafer surface become dominant, resulting in a tapered etching profile or etching that does not progress. For that reason, a low-

frequency power supply capable of generating high ion energy is generally used as a bias power supply. Also, according to Morikawa, CF_2 is the preferred radical contributing to the etching of silicon oxide films, and F radicals generated by excessive dissociation are known to reduce selectivity with respect to the resist and underlying film[4) to 6)]. For this reason, plasma sources that do not cause excessive dissociation of CF_4 gas are preferred. Additionally, deposits composed of C and F adhere to the sidewalls of the chamber as well as the wafer surface. These deposits cause selectivity with respect to the resist and underlying film to fluctuate, resulting in peeling and particle generation. To resolve such issues, measures must be taken such as a chamber structure that confines plasma only near the wafer, in-situ dry cleaning, and heating of chamber parts to reduce deposits. As described above, it is ideal for dielectric etching modules to be equipped with etching chambers designed to suppress excessive dissociation of fluorocarbon-based gases while also minimizing particle generation from C and F deposits.

3. Etching module overview

Our newly developed etching module (Fig. 1) employs a capacitively coupled plasma source with narrow electrode spacing—often referred to as a "narrow gap CCP"—which was widely used in the 1980s and 1990s. Its key features are as follows:

- It features a mechanism to adjust the position of the upper electrode.
- A 400 kHz high-frequency power supply is applied to the lower electrode.
- The wafer is processed by generating plasma at a narrow electrode spacing of approximately 10 mm.
- A confinement ring placed around the upper electrode periphery confines the plasma between the upper and lower electrodes.

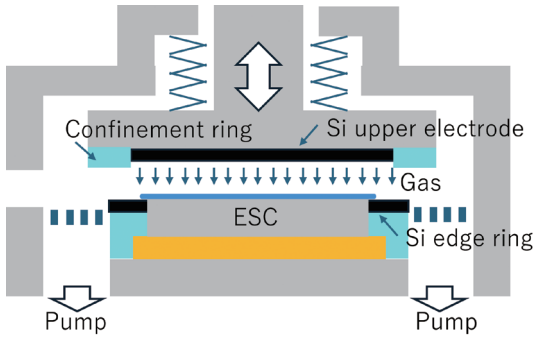

Fig. 1 Narrow gap CCP etching module

- It can be used with 6-inch and 8-inch wafers by replacing components inside the chamber.

Two separate chiller units, one pump unit and one power supply rack unit are connected to the etching module.

3.1 Lower electrode and exhaust of gases

The lower electrode is a ceramic electrostatic chuck (ESC) based on the ESC of Model NE and modified to support operation at a low frequency of 400 kHz. It is also equipped with a rear helium introduction system and a chiller-based cooling system to cool the wafer. The surface of the electrostatic chuck features a grooved design which, combined with the rear helium introduction system, provides excellent control of the in-plane wafer temperature. In addition, a ceramic electrostatic chuck electrode with high resistance to plasma is used to reduce the frequency of replacement and refurbishment.

Using insulating materials such as quartz for the edge ring installed around the wafer perimeter causes non-uniform sheath formation at the wafer edge, degrading the uniformity of both the etching rate and profile. To achieve a uniform sheath around the wafer perimeter, the edge ring is made of silicon material to which bias voltage is applied.

Also, to minimize any impact on uniformity, the process gas is exhausted isotropically via an exhaust distribution plate located around the bottom of the lower electrode, connected to an exhaust piping system consisting of four ports.

3.2 Upper electrode periphery and gas delivery system

The chamber's upper structure features a motorized mechanism for lifting and lowering the upper electrode. This lifting mechanism allows height adjustment in 0.1 mm increments during processing via the process condition setting screen, enabling compatibility with a wide range of processes. The upper electrode is grounded through this lifting mechanism.

When a low frequency of 400 kHz is applied to the lower electrode, a similar bias potential is also induced on the opposing upper electrode. Although the bias helps remove deposits composed of C and F adhering to the upper electrode, if an anodized aluminum base material is used for the upper electrode, the resulting aluminum fluoride (AlFx) may react with fluorine in the plasma to generate particles. Furthermore, elements such as Al and Mg contained in the Al base material may cause metal contamination. For this reason, a single crystal silicon electrode is used as the surface material of the upper electrode. This enables wafers to be processed in a chamber with minimal metal contamination and particle generation.

The upper electrode has numerous gas supply holes arranged in concentric circles. An 8-inch wafer-compatible device enables process gases to be introduced from separate gas boxes into the gas supply holes around the inner and outer periphery of the upper electrode. Each of these gas boxes has four mass flow controllers, allowing individual adjustment of gas flow rates for the inner and outer periphery of the upper electrode on the process condition setting screen.

4. Etching characteristics

The Model NE-5700 CCP used in these experiments was created by integrating this etching module with the transfer system of Model NE-5700. This system was employed to evaluate etching characteristics, wafer-to-wafer uniformity, and particle generation during operation.

4.1 6-inch wafer-compatible module

Fig. 2 shows the etching results for wafers with thermal oxide films processed using Ar, CF_4, and CHF_3 plasmas. A process pressure of 30 Pa and discharge power of 800 W were used, with a 1:1 flow rate ratio of CF_4 to CHF_3. The etching rate uniformity was ±2.4% within 2 mm of the wafer's outer periphery, achieving the target of ±5% or less. This result was achieved by optimizing the shape of the silicon edge ring and upper electrode to improve etching uniformity.

Subsequently, the wafer-to-wafer uniformity of etching characteristics and the particle generation were evaluated using a marathon running test. A 1:1.2 gas flow rate ratio of CF_4 and CHF_3 was used in this step. Because continuous operation on a mass production line is assumed, each lot was processed consecutively without performing plasma-based in-situ cleaning or maintenance involving opening the chamber. Silicon wafers were used for dummy wafers and particle measurements, with particles of 0.2 µm or larger being counted. Etching characteristics were confirmed using thermal oxide-coated wafers. To confirm the etching characteristics during the marathon running test, reproducibility was verified both within each lot and between lots. Because processing was performed on a lot-by-lot basis, etching characteristics were confirmed approximately every 2 hours during the first 8 hours of continuous discharge, and approximately every 8 hours thereafter.

Fig. 3 shows trends for the first lot used to confirm etching characteristics during the marathon running test. The etching rate was stable at approximately 420 nm/min., with wafer-to-wafer uniformity at that time being ±0.5%. The in-plane uniformity of the etching rate of each measured wafer was ±3% or better. Fig. 4 shows trends in etching rates and in-plane uniformity within the lots at the start of evaluation (0 hours) and after 74 hours of marathon running. The wafer-to-wafer uniformity of the etching rate within each lot was ±1.7%, with the in-plane uniformity of each wafer being ±2.8% or less. The etching rate within each lot showed a slight increasing trend regardless of continuous processing time, and uniformity also exhibited a slight increase. The eventual deterioration in uniformity observed after 74 hours of processing is attributed to wear of the silicon parts.

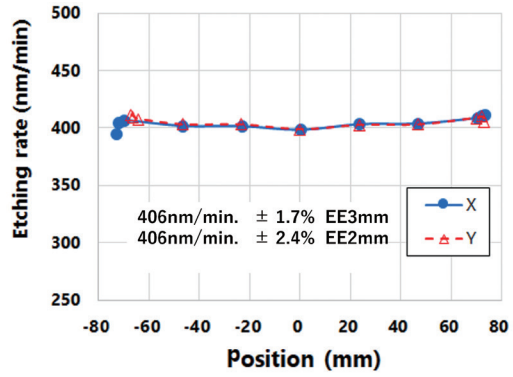

Fig. 2 SiO_2 etching rate and uniformity on 6-inch wafer

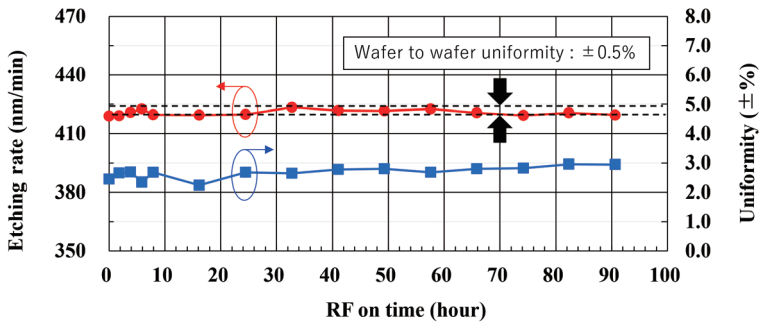

Fig. 3 Etching rate and uniformity in an 80-hour marathon running test

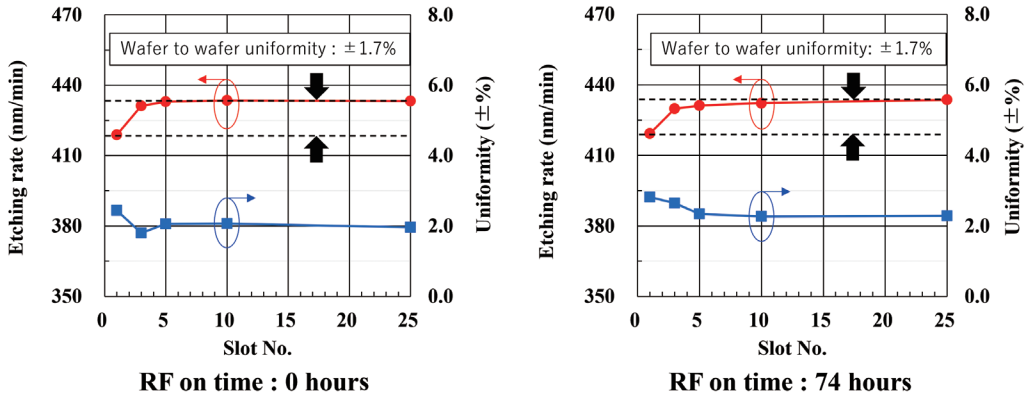

Fig. 4 Etching repeatability for one lot

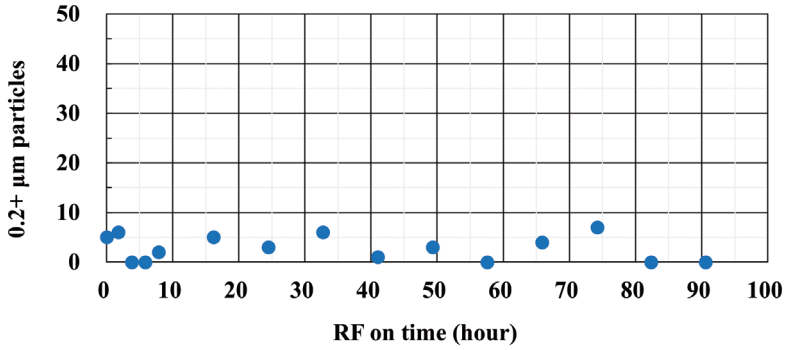

Fig. 5 Particle check results from 80-hour marathon running test

Fig. 5 shows particle measurement results. The particle count remained at 10 or below, achieving the targeted duration of 80 hours or more. After the marathon running test, the chamber was vented to the atmosphere and the condition of internal parts was inspected. The applied bias enabled the surfaces of the silicon upper electrode and edge ring to remain free of reaction byproducts and therefore retain their metallic luster. Although reddish-brown fluorocarbon deposits were observed around the lower electrode, no peeling was detected during visual inspection.

4.2 8-inch wafer-compatible module

Fig. 6 shows the etching characteristics of a typical 8-inch thermal oxide wafer. The processing conditions included a process pressure of 70 Pa, with Ar, CF_4 and CHF_3 used as process gases. As mentioned above, the upper electrode features a dual-line gas supply system and a gas ratio optimized to provide good in-plane uniformity of the etching rate. The in-plane uniformity of the etching rate within 4 mm of the wafer edge was approximately ±2%, achieving the target of remaining within ±5% regardless of the discharge power.

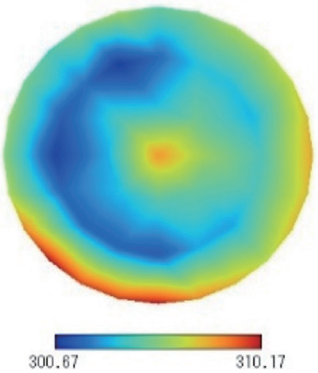

Fig. 6 SiO_2 etching rate and uniformity on an 8-inch wafer

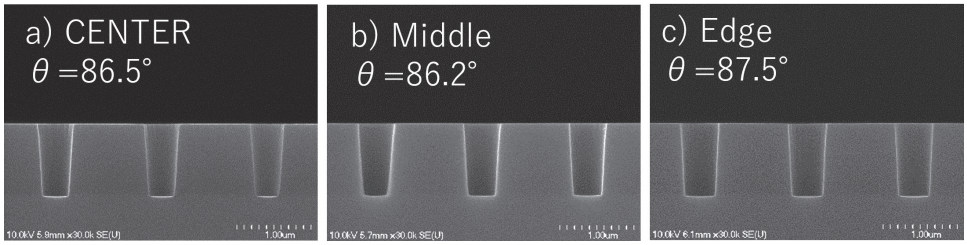

Fig. 7 Cross-sectional SEM images of 0.5 µm holes after 30% over-etching

Fig. 7 shows SEM images of 0.5 µm holes after 30% over-etching of the patterned thermal oxide wafer. The taper angle distribution calculated from each SEM image was within 1°.

5. Connectable transfer system

The etching module developed in this study will be mounted on the transfer core of the uGmni-200 model (Fig. 8), which allows the integration of multiple different process chambers such as etching, sputtering, ashing and CVD. The transfer core of the uGmni-200 is available in two configurations: a square transfer core that can accommodate up to two modules, and a hexagonal transfer core that can accommodate up to four modules. This flexibility enables compatibility with both small-scale and high-volume production.

6. Summary

This report presented a capacitively coupled plasma etching module specially designed for dielectric etching, capable of processing 6-inch and 8-inch wafers for electronic device manufacturing lines. This etching module provides excellent etching uniformity and wafer-to-wafer uniformity, and features a design that minimizes metal contamination and particle generation.

Fig. 8 uGmni-200 etching system

Because it can be connected to various transfer cores, we anticipate its application across a wide range of settings, from experimental lines to mass production lines. Although the current design is a narrow-gap capacitively coupled plasma etching module with a 400 kHz high-frequency power supply, it is compatible with power supplies of different frequencies, enabling use in a wide range of processes.

By supporting the electronics industry with our technology, we hope to contribute to realizing a more prosperous, safe, and secure future.

References

1) S. Shinohara: JSPA Catalog No. AP992339, JSAP, Tokyo (1999), p. 1.
2) M. Sekine : J. Plasma Fusion Res. **83**, 319 (2007).
3) T. Tatsumi: Oyo Buturi **85**, 761 (2016).
4) Y. Morikawa: (2003). Study of Dry Etching Technology Based on Gas-Phase and Surface Reaction Control [Doctoral dissertation, Graduate School of Engineering,The University of Tokyo].
5) M. Yoneda: (1998). Study of Applications for Plasma Etching Technology in Semiconductor Devices [Doctoral dissertation, Kyoto University Graduate School of Engineering Faculty of Engineering].
6) T. Tatsumi, H. Hayashi, S. Morishita, S. Noda, M. Okigawa, N. Itabashi, Y. Hikosaka, and M. Inoue: Jpn. J. Appl. Phys., **37**, 2394 (1998).