# Filling Technology of Insulating Layers by Phase Position Control

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When radio frequency (RF) power sources are used on both the cathode and stage sides, effective stage bias can be achieved by controlling the RF phase. We found that this can be ascertained from the voltage peak to peak (Vpp) curve at each phase position.

The number of layers in 3D-NAND flash memory is increasing, so the processed height of each layer must be reduced to maintain the total device height. The height of etch-stop layers must also be reduced, and a filling process is required for insulator materials. ULVAC had knowledge of stable RF sputtering processes, but we were not able to produce an adequate filling performance. We knew that the stage bias process used in conventional ULVAC technologies, such as high coverage ionized sputtering (HiCIS), was a good candidate for this filling process. However, it is only used for metal layers, which have lower ionized energy materials. We tried to combine both cathode and stage RF processes, but the filling performance was not stable and we could not control the RF processes together. In order to solve these issues, we found that phase control is one of the key factors to not only use matching control but also control stage bias effectiveness. Also, filling performance can be controlled by selecting the correct phase position for both the cathode and stage RF output. It makes further possibility for sputter process applications.

### 1. Introduction

Traditionally, NAND flash memory has a structure in which memory cells are arranged horizontally on a semiconductor substrate, and its memory capacity was able to increased by miniaturizing these memory cells.

On the other hand, there is Physical limitation for cell size miniaturization. Thus, 3D-NAND flash memory was developed to improve per-chip storage capacity by stacking memory cells vertically.

One of the technical challenges in 3D-NAND flash memory is the etching technology to form channel holes that penetrate the multiple layers of film. In order to etch multilayers uniformly, in some cases, an insulating layer that has high etching resistance and is suitable for mass production is preferred as the bottom layer.

ULVAC has long provided RF sputtering technology which represented as an insulating layer deposition technology<sup>1.4</sup>, and has already delivered a number of equipments to mass production plants as hard-mask and etch-stop layers (ESLs) technologies.

\*1 Semiconductor Equipment Division, ULVAC, Inc. (1220-14 Suyama, Susono, Shizuoka 410-1231, Japan) Recently, the number of layers in 3D-NAND flash memory has keep increasing with each successive generation. Therefore, in addition to reducing the height of each memory layer, it is necessary to develop a technology to deposit thinner and more uniform ESL layers as described above. Furthermore, a technique to fill the within the pattern is required for these insulating layers.

The conventional RF sputtering technique, in which a film is deposited only by the cathode side process, has a dificculty for filling. Furthermore, the technique requires introducing radio frequencies into the substrate side, but technical issues must be solved in order to handle multiple RF power sources at the same time.

As a result of repeated experiments to solve this problem, we found that more effective substrate bias can be achieved by controlling the phase position. This paper introduces a technique for filling trench patterns by using this insulating layer sputtering process.

# 2. Features of ULVAC's RF sputtering system

One of the layers required for the 3D-NAND process is the Al<sub>2</sub>O<sub>3</sub> layer, which has excellent etching resistance and can be quickly removed by chemicals after patterning. The sputtering process, which has a relatively high sputter rate and good film thickness uniformity, is used to make this insulating layer. For the evaluation result reported in here, we used the ENTRON-EX W300, a multi-chamber sputtering system equipped with a module dedicated to RF sputtering using radio frequencies. The system is configured for 300 mm size wafers and is equipped with features to achieve high throughput and low particle counts suitable for mass production of semiconductor memory. In addition to the above, the process chamber has the following features.

- (1) By spray coating on the side surface of the Al<sub>2</sub>O<sub>3</sub> target with an optimum material film, it is possible to prevent abnormal discharge (arcing) that occurs during RF output, suppress particles, and ensure process stability<sup>4</sup>.
- (2) The system uses the RFS1350LH process power supply, which has a function for detecting and instantaneously stopping the output of microarcs before large arcs are generated during the process (microarc cut function), thus preventing the occurrence of particles.
- (3) The unique chamber configuration enables stable insulating layer deposition because a ground potential can always be present even if the insulating layer is continuously deposited<sup>2</sup>).
- (4) A labyrinth structure is used to prevent plasma leakage, which is a cause of instability, even when high RF power corresponding to 300 mm wafers is output<sup>3</sup>). This allows the output of 13.56 MHz radio frequency in the range of 100 W to 5000 W, ensuring a sputter rate suitable for mass production.

# 3. Filling technology challenges and solutions

#### 3.1 Challenges in insulating layer filling technology

Using an RF sputtering process has made it possible to deposit an insulating layer in a stable manner. However, this deposition method was established as a technique for depositing films on flat surfaces, and challenges remain for filling in patterns on substrates such as holes and trenches.

There have several sputtering processes that have improved coverage for these patterns as discribed as long through sputtering (LTS), self-ionized sputtering (SIS), and high coverage ionized sputtering (HiCIS)<sup>5)</sup>. However, all of these are sputtering technologies for metal targets and cannot be applied to the insulating layer sputtering process. We therefore tested a sputtering process that improves filling performance by supplying RF power to both the sputtering target and substrate with controlling the phase of the output RF. The filling characteristics of the insulating layer formed by this deposition method<sup>6)</sup> may change depending on the phase of the RF power supplied to the substrate, so it is important to know the optimal conditions that improve these characteristics.

### 3.2 Equipment configuration to achieve insulating material filling deposition

Fig. 1 shows a schematic diagram of the chamber configuration in which this evaluation was carried out. To implement the insulating layer sputtering, the RF power supply 1 (RF1) is connected to the cathode electrode side including the target, and the other RF power supply 2 (RF2) is connected to the stage side where the substrate is mounted in order to fill Al<sub>2</sub>O<sub>3</sub> into the pattern by repeated etching and resputtering. Since the phase of the RF output from each power source is adjusted by the phase controller, it is possible to adjust the phase difference of each output even when using RF power supplies of the same frequency. Fig. 2 shows the waveforms actually output from each power supply. The output radio frequency is read by an oscilloscope from the positions of Pickup 1 and Pickup 2 shown in Fig. 1. The figure shows how the waveform output from RF2 is shifted by changing the phase difference.

In addition, each power supply is equipped with an independent matching circuit (matching box), which enables to make stable RF output by automatically adjusting the resistance values of Tune (C1) and Match (C2).

## 3.3 Features and controls when using multiple RF power supplies

To evaluate the deposition of the Al<sub>2</sub>O<sub>3</sub> layer, we set the RF outputs to 4000 W and 400 W on the cathode side and stage electrode side, respectively, introduced 200 sccm of Ar gas, and conducted the discharge with the chamber pressure regulated to approximately 2 Pa. On the cathode electrode side, we used the magnetron sputtering method to deposit Al<sub>2</sub>O<sub>3</sub> as the target material by discharging while rotating the magnet circuit at a constant speed.

Fig. 3 shows the variation of the voltage peak to peak (Vpp) value obtained when the phase position of the RF2 power supply is moved, and the variation of the C1 and C2 values of the RF2 power supply at the matched positions. Here, the Vpp value is obtained by reading the voltage on the output side of the matching box.

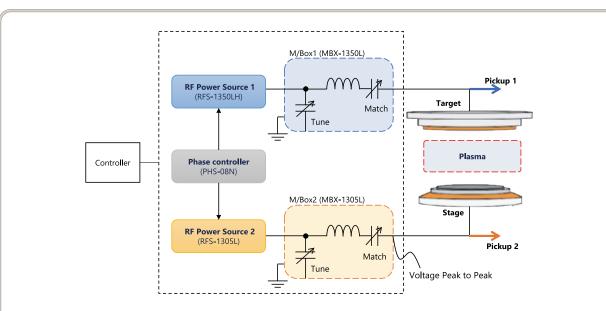
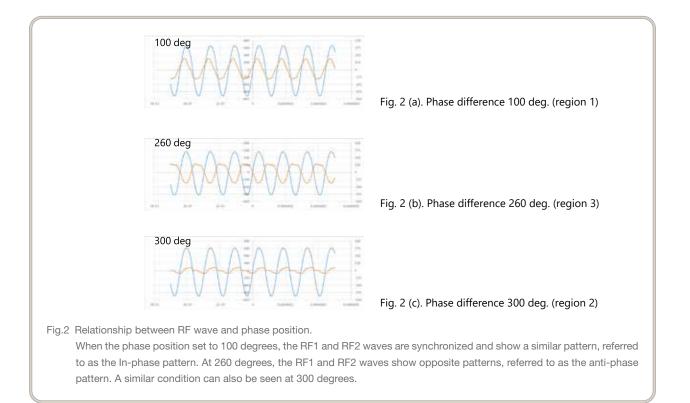
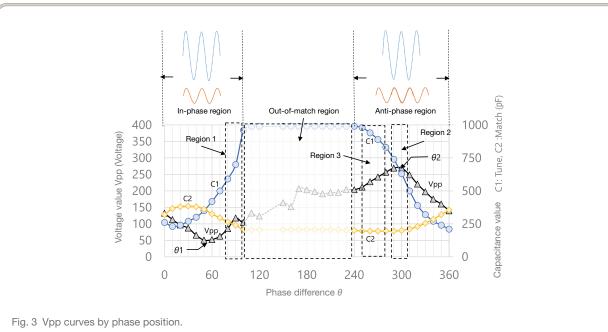


Fig. 1 Schematic of chamber configuration and process power supply control. RF1 is connected to the cathode electrode, which has the sputtering target, and RF2 is connected to the stage electrode, which has the substrate. Each power supply is connected to the phase controller and the wave point is controlled by phase. The RF bias process is controlled in the matching box with impedance control for Tune (C1) and Match (C2).
Each RF wave is monitored by an oscilloscope from Pickup 1 and Pickup 2. The RF2 voltage peak to peak (Vpp) value is monitored at the output point of the matching box.



The graph shows that as the phase difference changes, the Vpp values assume a concave shape that bottoms out at around 50 degrees (labeled  $\theta$ 1). The C1 value, in contrast, continues to rise as the phase difference increases, and once the phase difference exceeds 100 degrees, the discharge can no longer be maintained.

Next, when the phase difference was changed in the opposite direction and the output of RF2 was decreased



Vpp shows a concave curve from phase 0 to 100 degrees and a convex curve from phase 240 to 360 degrees. From the process data, we refer to 80-100 degrees as the effective bias zone (Region 1), 290-310 degrees as the other effective bias zone (Region 2), and 250 to 280 degrees as the too-effective bias zone (Region 3).

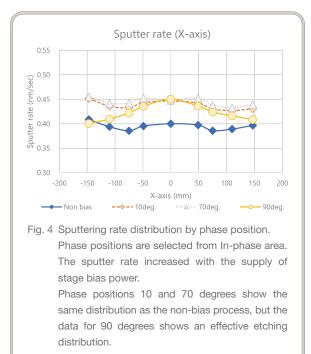
starting from 360 degrees, the Vpp values assumed a convex shape with a peak near the phase difference of 300 degrees (labeled  $\theta$ 2). Here, the C1 value rises with the decrease of phase difference, and discharge cannot be maintained in a range lower than 240 degrees of phase difference.

Based on the relationship between the above results and the waveforms obtained from Fig. 2, the range of phase differences from 0 to 100 degrees is called the in-phase region, the range of phase differences from 240 to 360 degrees is called the anti-phase region, and the remaining region where plasma cannot be maintained stably is called the out-of-match region.

## 3.4 Deposition performance at different phase positions

Next, we will discuss the changes that occurred during actual deposition in these regions. Fig. 4 shows the in-plane film thickness distribution in the x-axis direction, plotted as the sputter rate at different positions, when deposition was performed in the in-phase region defined above. The horizontal axis shows the measured position, and the vertical axis shows the sputter rate at each measured position.

The condition in which RF is not output to the substrate electrode side, called the "non bias" condition, is shown as the reference standard sputtering rate. The same output



was used for each of the other deposition plots in the figure, varying only the phase position.

The sputter rate exceeded the non bias reference standard under every phase position condition. This is thought to be because the Ar<sup>+</sup> in the deposition chamber was incorporated

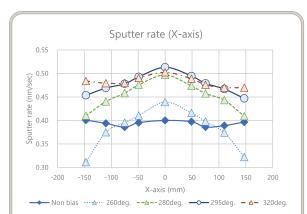
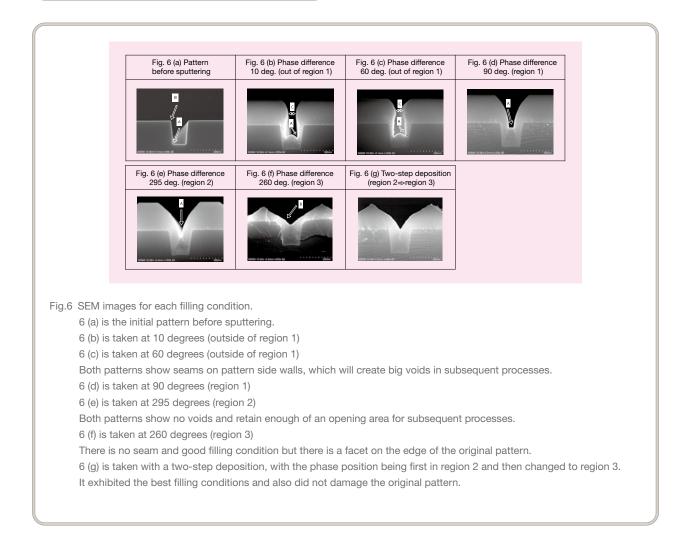


Fig. 5 Sputtering rate distribution by phase position. Phase positions are selected from the anti-phase area. As in the in-phase area, the sputter rate increased with the supply of stage bias power. The 295 degree condition shows similar performance to the 100 degree condition in the in-phase area. At 280 degrees and 260 degrees, greater etching effectiveness is seen at lower phase positions.

into the film due to the RF output on the substrate side. Comparing sputter rate distributions, under the 10 degree and 70 degree phase difference conditions, the overall sputter rate increased without a change in the shape of the distribution. In contrast, under a phase difference of 90 degrees, the shape of the distribution changed, revealing enhanced etching effectiveness particularly at the outer periphery of the substrate.

In other words, the figure shows that it is possible to change the deposition performance by changing the phase position at which the RF power is introduced. Based on these results, we defined region 1 as the phase difference range where the substrate bias is effective in the range extending 30 to 50 degrees from  $\theta$ 1, which marks the lowest Vpp value in the in-phase region.

Fig. 5 shows plots of the sputter rates when deposition was performed in the anti-phase region. In the anti-phase region, a phenomenon similar to the in-phase region occurs. When sputtering at 320 degrees, the sputter rate increases without a change in the shape of the in-plane distribution, whereas at or



53

54

below 295 degrees, the etching effectiveness is apparent. The change in the distribution shape becomes larger as the phase position is lowered, with the distribution shape changing significantly under the 260-degree condition.

Based on these results, we defined region 2 as the range spanning 10 degrees before and after  $\theta 2$ , which marks the highest Vpp value in the anti-phase region. Furthermore, we defined region 3 as the part of the anti-phase region at phase positions lower than region 2 where etching effectiveness was observed.

#### 3.5 Filling characteristics by phase region

These results demonstrate that the deposition performance can be significantly changed by changing the phase position; that is, the deposition state can be changed. Next, we evaluated the filling characteristics of the films deposited under these conditions.

Fig. 6 (a) to Fig. 6 (g) are cross-sectional scanning electron microscope (SEM) images. Fig. 6 (a) shows the pattern before sputtering. We carried out the filling evaluation using a recessed pattern with a depth of 240 nm and aspect ratio of 1.0 composed of silicon oxide. The area indicated by arrow A is the edge where the bottom and side walls intersect at 90 degrees, and the area indicated by arrow B is the very top of the side wall. Fig. 6 (b) to Fig. 6 (g) are cross-sectional SEM images of the sputtered film after the Al<sub>2</sub>O<sub>3</sub> layer was formed in the recessed pattern.

Fig. 6 (b) and Fig. 6 (c) show the results of sputtering in the in-phase region at phase differences of 10 degrees and 60 degrees, which are outside of region 1. The figures show that when the sputtering was carried out under these conditions, the coverage of the  $Al_2O_3$  film out to the edges indicated by arrow A was not good, leaving sharp-angled seams at the edges. Furthermore, the opening indicated by arrow C was constricted, which means continued deposition would close up the top of the opening and leave a void inside.

In contrast, when sputtering was performed at a phase difference  $\theta$  belonging to region 1, for example at a phase difference of 90 degrees as shown in the SEM image in Fig. 6 (d), there were no sharp-angled seams at the edges of the Al<sub>2</sub>O<sub>3</sub> layer. In this case, the filling characteristics of the Al<sub>2</sub>O<sub>3</sub> film were excellent.

We also confirmed these results for shallower geometries with aspect ratios of 0.2 to 1.0. Next, we checked the filling characteristics in the antiphase region.

Fig. 6 (e) shows the SEM image when sputtering was performed with a phase difference of 295 degrees, which is inside region 2. In this case, just as in Fig. 6 (d), an  $Al_2O_3$  layer with excellent filling characteristics was formed.

Meanwhile, as an example of sputtering in region 3 in which the etching effectiveness is further enhanced, Fig. 6 (f) shows the result of sputtering with a phase difference of 260 degrees.

In this case, although the filling characteristics were excellent, the etching effectiveness was so strong that it etched the uppermost edge of the recessed pattern, indicated by the arrow B, breaking the original pattern.

We thought that a solution to this problem might be to perform sputtering in region 2 and then switch the phase position to region 3 in the middle of the sputtering.

Fig. 6 (g) shows the results when sputtering was performed in region 2 and then the phase position was switched midway to region 3. This two-step deposition process made it possible to obtain superior filling characteristics without damaging the pattern on the substrate.

### 4. Summary

We were able to demonstrate that when depositing an insulator into a pattern on a substrate in this manner, even if both RF power source 1 for sputtering and RF power source 2 for applying stage bias have fixed power, manipulating the phase difference  $\theta$  changed the deposition characteristics of the film and also changed the filling characteristics of the film into the recessed pattern.

Furthermore, since these characteristics can be determined by reading changes in the Vpp values obtained during discharge, it is possible to confirm the appropriate processing conditions from the parameters during deposition. We therefore expect this technique to greatly expand the possibilities for mass production adaptation of the insulator filling process using RF sputtering.

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