Low-damage Dry Etching Technologies for GaN Power Devices

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Presented in this report are low-damage dry etching technologies for Gallium nitride (GaN) power devices using inductively coupled plasma reactive ion etching (ICP-RIE) equipment with a newly-developed high-frequency RF power supply. GaN vertical trench-gate metal-oxide-semiconductor field-effect transistors (MOSFETs) are promising devices for realizing high-breakdown voltage and low on-resistance. However, generally, when a trench-gate structure is fabricated by ICP-RIE, these properties degrade due to plasma-induced damage which is formed near the GaN surface. Our RF power supply contributes to the reduction of this damage by outputting accurately-controlled and ultimately-low bias power. This report introduces an overview of the RF power supply and recent achievements using the same.

1. Introduction

This work includes results supported by grant No. JPJ005357 to Nagoya University as a cooperating organization of the "Research and Development of Next Generation Semiconductors to Realize an Energy-saving Society" program through the Ministry of Education, Culture, Sports, Science, and Technology (MEXT).

This project aims to accelerate research and development for the practical application of gallium nitride (GaN), a promising next-generation semiconductor material, by establishing an R&D center that integrates research and development from material creation to device operation verification and system application, and by conducting basic research using theory and simulations.

With the rapid progress of science and technology in recent years, energy consumption is growing significantly worldwide. Meanwhile, carbon dioxide (CO_2) and other greenhouse gases emitted from energy generation and gasoline vehicles are having a significant impact on the environment. Research and development aimed at preventing global warming and conserving energy is therefore very important and has become an urgent priority. Compared to silicon (Si), which is currently the mainstream material for semiconductor power devices, GaN has superior fundamental properties such as a higher band gap energy, higher breakdown field strength, and higher electron mobility. GaN is therefore expected to be used in low-loss, high-voltage power devices, especially in hybrid electric vehicles (HVs) and electric vehicles (EVs), which have a smaller environmental footprint.

Research and development is underway on a range of element structures for power devices using GaN [1]. These include vertical trench-gate metal-oxide-semiconductor field-effect transistors (MOSFETs), which have been attracting attention as devices that enable chip miniaturization and high-speed switching due to their unique device structure. As the name "trench-gate" suggests, a groove (trench) with a width and depth of about 1 μm is formed in the surface of a GaN wafer to function as a gate for switching the device on and off.

The trench is formed by an etching process. Its sidewall serves as a pathway for electrons to flow as an inversion layer during device operation. Therefore, etching techniques that can form trenches with good verticality and sidewall surface flatness are essential to improving the device evaluation metrics, especially channel mobility. Another important issue is how to reduce the damage to the GaN introduced during trench formation.

In this paper, we present recent efforts by ULVAC to control GaN trench shape and reduce damage, and the results thereof.

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2. GaN Dry Etching Technology

2.1 Trench forming technology

Typically, inductively coupled plasma reactive ion etching (ICP-RIE) is used to fabricate the trench structure.

The main piece of ICP-RIE equipment used in this study is the NE-550EX etching system, which is part of ULVAC's standard lineup (Fig. 1).

ICP-RIE, whose advantages include its ability to use high-density plasma and its simplicity of plasma control, is often used for the etching of GaN, which is considered to be a particularly difficult material to process [2,3].

Chlorine gas is used as the reactive gas for GaN etching. By optimizing the chlorine gas used to control the trench shape, we were able to successfully form trenches with good verticality and sidewall flatness [4].

Fig. 1 ICP-RIE equipment, NE-550EX

Fig. 2 shows an example of the trench shape observed by electron microscopy (SEM). The figure shows a good vertical trench with a tapered angle of almost 90°. We also measured the surface roughness of the trench sidewall and were able to confirm a good flatness with a surface roughness Sq of about 1 to 2 nm.

On the other hand, since the ICP-RIE etching technique uses reactive ions to physically and chemically react with the sample surface, it leaves the GaN surface layer susceptible to damage caused by ion impacts and other plasma-induced damage.

The damage is known to induce disordered bonding and the formation of defective levels in the GaN crystals [5], and there have been concerns that this will lead to the degradation of the device characteristics mentioned earlier.

Therefore, in order to reduce the damage caused by ICP-RIE GaN etching, we focused on bias power (P_{bias}), which is one of the processing parameters considered to be particularly related to ion impacts.

2.2 Low-damage etching technology

In ICP-RIE, P_{bias} is supplied by a high frequency RF power supply (12.5 MHz) connected to the lower electrode and matching box (M/B). In this study, in order to control extremely low P_{bias} below 5.0 W with high accuracy, we equipped the NE-550EX with a dedicated unit that includes serial communication capability, a high-precision RF power supply with output calibration in 0.1 W increments, and a high-precision M/B with enhanced sensors and improved matching accuracy. Using this dedicated unit, a rise time of 5 msec and output fluctuation of +/-0.25% were achieved at an output of P_{bias} = 3.0 W.

This made it possible to maintain a precisely controlled state with little output error for a long time with a P_{bias} as low as 0.1 W.

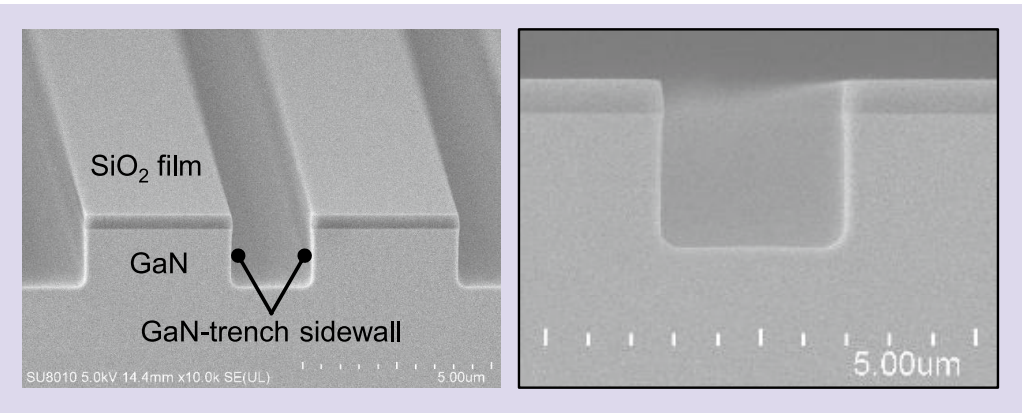

Fig. 2 Example of GaN trench structure fabricated by ICP-RIE

This dedicated unit has already been released, and we hope that it will be used for etching not only GaN but also various other materials in the future.

2.3 Demonstration of low GaN damage

To evaluate the GaN etching damage, it is common to examine the electrical characteristics of Schottky barrier diodes (SBDs) fabricated on the etched surface [6-8].

We fabricated Ni/n-GaN SBDs (Fig. 3) on an n-type GaN epitaxial layer on a GaN substrate (Si concentration: 5 × 11016/cm3) having ohmic electrodes vapor-deposited on the back surface thereof by etching the surface of the crystal-grown sample at Pbias values ranging from 2.5 to 60 W and then vapor depositing nickel (Ni) Schottky electrodes onto the n-type GaN epitaxial layer.

Fig. 4 shows the forward *I-V* characteristics of these SBDs. The figure shows that the barrier height (Φ_B) of the GaN Schottky decreases as P_{bias} increases more than in an unetched (as-grown) Schottky.

This is thought to be due to the introduction of a damage layer with the formation of defect levels near the GaN surface by the etching process, indicating that the reduction of P_{bias} is important for reducing damage. However, in general, the etching rate decreases as P_{bias} is reduced, which means that low P_{bias} processing alone is impractical, especially for trench formation processes that require etching depths on the order of microns.

Therefore, we have developed a multi-step bias power etching technique that enables both low damage and high etching rates.

Our technique involves high P_{bias} processing followed by low P_{bias} processing, with the aim of using the low P_{bias} processing to eliminate the damage layer introduced by the high P_{bias} processing.

In fact, in similar SBD evaluations, we were able to confirm the low damage effects of this technique , and we found that the layer of slight damage remaining after the low P_{bias} processing could be restored by heat treatment (annealing) [9,10].

We are also applying this technology to trench structures, and have confirmed that our multi-step bias power etching technique is effective at improving the channel mobility of MOSFET devices [11].

3. Summary

We have developed a trench formation process and a low-damage etching system, which are key processes for realizing GaN power devices for use in environmentally friendly electric vehicles, a market that is expected to expand in the future.

The NE series dry etching system used in this study has a proven track record not only for precise control of P_{bias} by means of the high-precision RF power supply introduced in this study, but also for in-plane uniformity of processing dimensions, and can be expected to support a variety of materials and applications in the future.

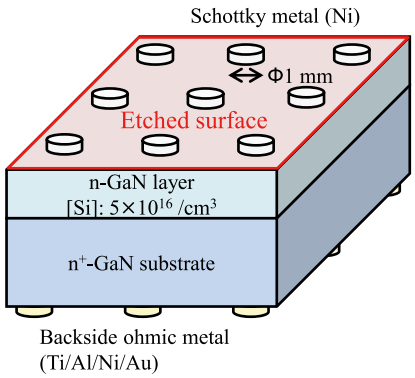

Fig. 3 Schematic view of Ni/etched n-GaN Schottky barrier diode structure

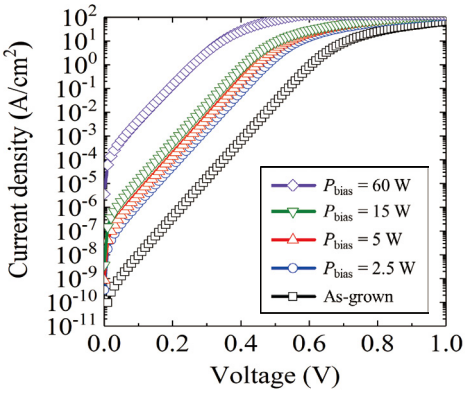

Fig. 4 *I–V* characteristics of SBDs with different dry-etching conditions in forward bias voltage

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