Deposition Technology for Cu Interconnect of Semiconductor Devices

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We have developed pre-treatment, Cu sputtering, and CVD-Co technologies for semiconductor Cu interconnect technology. A new remote plasma process in the pre-treatment technology suppressed damage to low-k films, and uniformity in the wafer surface and stability of continuous treatment were obtained. The new CVD-Co process enabled uniform film formation at a film thickness of 1.5 nm and resulted in good step coverage performance in a fine pattern. In the future, we expect that these interconnect formation technologies will be applied in logic and memory devices.

1. Introduction

In recent years, LSIs (Large Scale Integrated Circuits) have been installed not only in personal computers and smartphones but also in home appliances and automobiles, and have become important as the basis of semiconductor devices for the realization of an IoT (Internet of Things) society where all things are connected via the Internet. It is well known that LSIs have continued to increase in density through miniaturization in accordance with Moore's Law. As shown in Fig. 1, the metal wiring of such a circuit has a three-dimensional multilayer structure to connect the transistors on the Si substrate. As of 2020, the minimum wiring width in the lowest layer of Cu interconnects has been reduced to 20 nm, and materials such as metal wiring using Cu or CVD-Co and interlayer dielectrics using SiO_2 or low-k materials are being developed for further miniaturization[1].

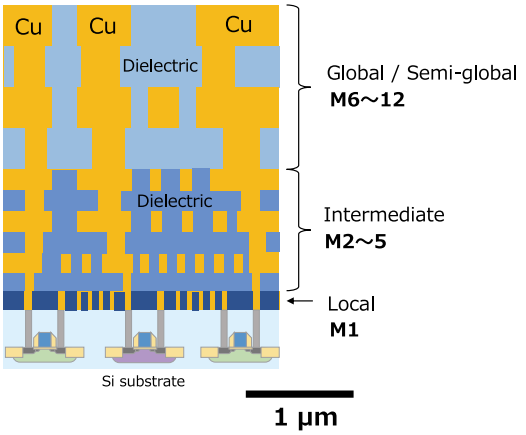

Fig. 1 Cu interconnect cross section

We have developed several Cu interconnect technologies for semiconductor devices, including pre-treatment technology, Cu sputter deposition technology, and CVD-Co deposition technology for cutting-edge wiring materials. In this paper, we introduce our pre-treatment, Cu sputtering, and CVD-Co technologies for next generation Cu interconnects, all of which are used in our ENTRON-EX sputtering system for semiconductor devices.

2. Pre-treatment Technology: Remote Plasma

2.1 Background

A Cu interconnect in a semiconductor device is formed by filling conductive materials into trench grooves and via holes (dual damascene structure) etched in the interlayer dielectric. The conductive materials are formed by first depositing a barrier layer (Ta/TaN) and seed layer (Cu) by sputtering, followed by electrolytic plating to implant Cu, and then chemical mechanical polishing (CMP) to planarize the metal. By repeating these processes, the semiconductor Cu interconnect is constructed. A native oxide film of the Cu is present on the top surface of the Cu interconnect. Because this Cu oxide film increases the contact resistance between wiring and adversely affects the device characteristics, a technique for removing the oxide film before the sputtering process is necessary. In the past, hydrogen ions were generated by inductively coupled plasma (ICP) and then drawn into the substrate by applying RF substrate bias to reduce the Cu oxide film. In recent years, low-k materials have become the dominant material for interlayer dielectrics

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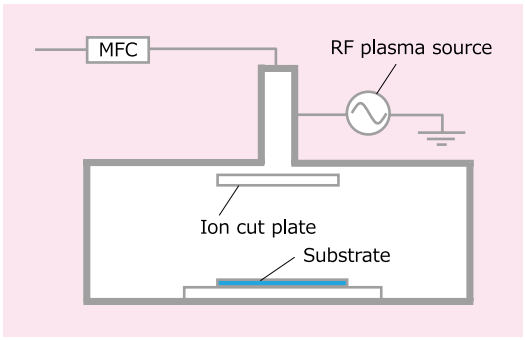


Fig. 2 Schematic of remote plasma apparatus

in order to support miniaturization.

However, the problem is that low-k materials are sensitive to hydrogen ions, which causes the dielectric constant to increase. Therefore, it is necessary to perform a pre-treatment technology capable of suppressing damage to the low-k material while reducing the Cu oxide film. To this end, we developed a remote plasma technique using hydrogen radicals to shield hydrogen ions by isolating the plasma source from the wafer processing chamber (Fig. 2).

2.2 Conditions required for hydrogen radicals to reach wafer

Hydrogen radicals have a short lifetime for recombination and are easily deactivated. One of the reasons for deactivation is that the hydrogen radicals collide with the surface of the chamber walls and inner parts of the equipment. As a countermeasure, it is important to use materials suitable for hydrogen radicals. The suitability of the material depends on its recombination coefficient[2]. The recombination coefficient of oxygen-terminated surfaces is lower than metal surfaces. Adding oxygen gas to processing gas is also effective in increasing the lifetime of the hydrogen radicals, likely because the addition of the oxygen results in oxygen termination of the surface of the chamber walls and inner parts. However, there is concern that the oxygen will remove the methyl groups from the low-k film used as the interlayer dielectric[3]. When a methyl group, which is a hydrophobic group, is removed, water is easily adsorbed and causes an increase in the k value of the low-k film. Therefore, it is also important to control the oxygen supply.

2.3 Evaluation of reduction on the surface of the Cu film

We evaluated reduction by using CuOx, a native oxide layer in Cu films. In the evaluation procedure, a 60 nm sputtered Cu film was deposited on a thermally oxidized Si wafer and then exposed to air to form the CuOx film on the Cu surface. The substrate with this CuOx film formed

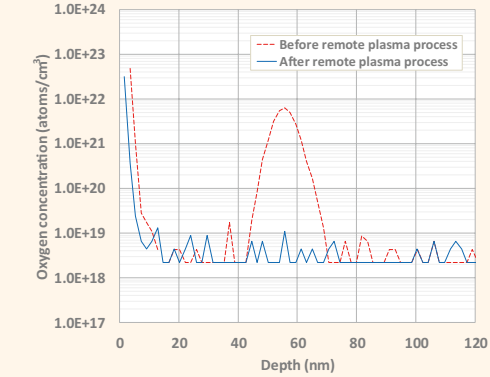


Fig. 3 SIMS profile of Cu/Cu/SiO_2 sub

on the top surface was reduced by a hydrogen radical treatment using remote plasma, and then the sputtered Cu film was deposited to 60 nm in-situ. This resulted in a film composition of Cu (60 nm) / CuOx / Cu (60 nm) / thermal SiO_2 film, and rendered the CuOx layer as a remote plasma-treated film. The oxygen concentrations of samples with and without reduction processing were compared by SIMS analysis.

Fig. 3 shows the SIMS analysis results. Without reduction processing, the oxygen concentration was about 5E+21 atoms/cm³ in the thickness range of 40 nm to 70 nm in the Cu film. Meanwhile, when reduction processing was performed, the oxygen concentration peak in the same thickness region of the Cu film was reduced to the oxygen concentration of the sputtered Cu film. This indicates that the CuOx was reduced and oxygen was removed by hydrogen radicals generated by remote plasma.

2.4 Evaluation of low-k dielectric constant in CuOx reduction conditions

Next, we evaluated the change in the dielectric constant of the low-k film in the reduction conditions. Black Diamond IIx, a silicon-based (SiOC) low-k film manufactured by Applied Materials, was used as the evaluation sample. After the hydrogen radical treatment with remote plasma, the dielectric constant was measured on the surface of the low-k substrate by using a mercury prober. Table 1 shows that the k values before and after reduction processing are both in the range 2.5 to 2.6, indicating almost no change in the dielectric constant of the low-k film before and after reduction processing.

Table 1 Dielectric constant of low-k film

	Before remote plasma process	After remote plasma process
Low-k value	2.59	2.57

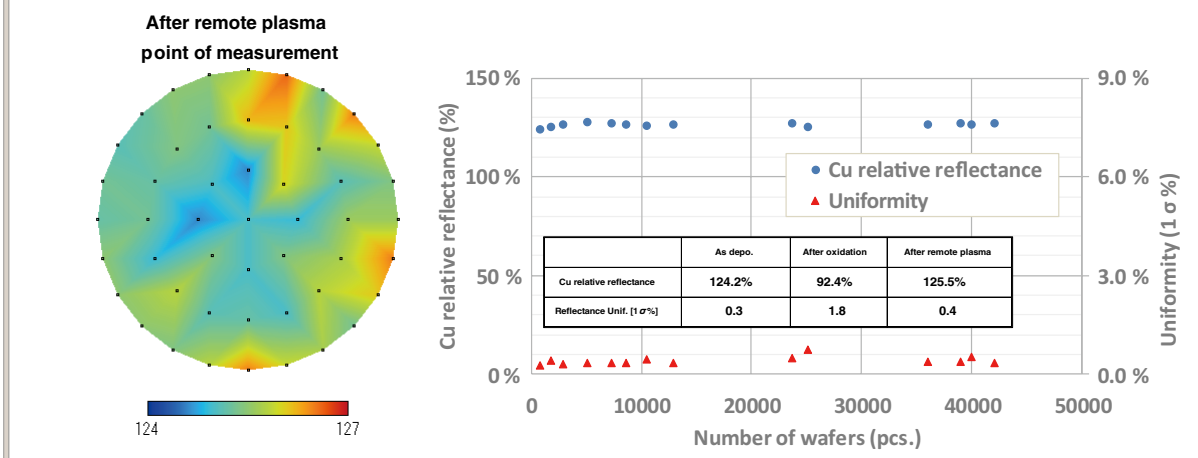


Fig. 4 Cu or CuOx relative reflectance and uniformity

2.5 Evaluation of in-plane uniformity and stability of remote plasma

In order to evaluate the in-plane uniformity and stability of the reduction processing, reflectance was measured by using a 300 mm diameter wafer formed with a Cu oxide film.

- Optical wavelength: 436 nm
- Measurement points: 49 points edge cut 3 mm
- Relative reflectance: Cu reflectance/bare Si wafer reflectance
- Number of wafers: 1 to 40,000 pcs.

Fig. 4 shows the relative reflectance and the in-plane uniformity and stability of reduction processing. After continuous processing equivalent to 40,000 wafers, stable results were obtained in terms of Cu relative reflectance and uniformity.

3. Cu Sputtering Technology

We used the SIS (Self Ionized Sputtering) technique to provide uniform step coverage to fine patterns[4]. This technique improves step coverage by increasing Cu ions generated by self-ionized discharge and then drawing the Cu ions into the wafer by using mechanisms that control spatial electric and magnetic fields and applying a negative bias to the wafer. Fig. 5 shows a schematic diagram of the apparatus. The apparatus is equipped with a mechanism to apply a positive voltage to the shield inside the sputtering

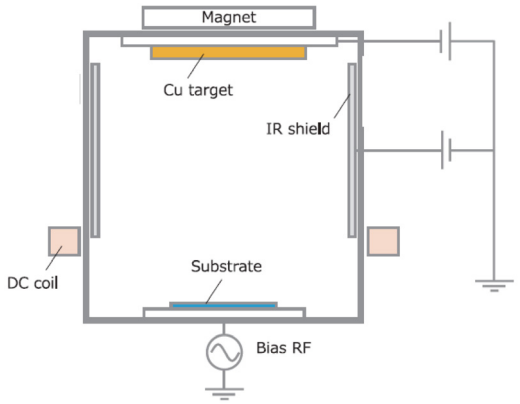
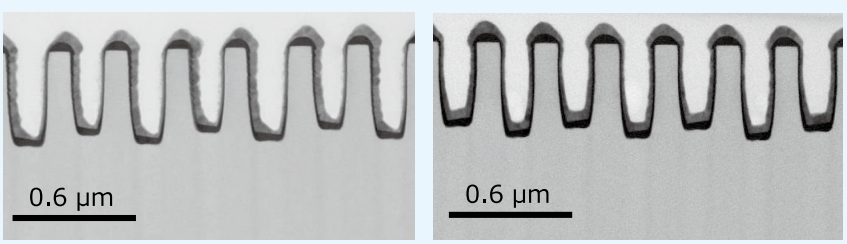


Fig. 5 Schematic of Cu sputtering apparatus



(a) w/o magnetic field control **(b)** w/ magnetic field control

Fig. 6 Comparison of coating characteristics of Cu film with and without controlling the spatial magnetic field

chamber and a mechanism to generate a magnetic field in the space inside the sputtering chamber by means of an electromagnet coil outside the chamber. This allows Cu ions that have escaped to the periphery to be collected, increasing the quantity of ions supplied to the wafer and enabling the Cu ions to enter the wafer vertically.

Fig. 6 shows the step coverage results of Cu sputtering on the patterned substrate with and without control of the spatial magnetic field. When the spatial magnetic field is not controlled, a large number of sputtered Cu particles are introduced to the patterned substrate from the direction of the center of the wafer. As a result, the thickness of the Cu film on the sidewalls is asymmetrical from left to right, and the Cu film on the bottom of the via holes has a sloped shape. Poor step coverage can cause voids in the subsequent electro-plating process, resulting in electromigration problems. Meanwhile, by controlling the spatial magnetic field, the directionality of the Cu ions is improved and a Cu film with symmetrical sidewalls and flat via hole bottoms is formed, indicating better step coverage.

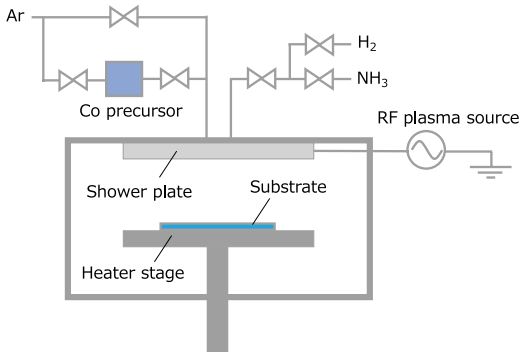


Fig. 7 Schematic of CVD-Co apparatus

4. CVD-Co Technology

CVD-Co liners are used in Cu interconnects of cutting-edge logic devices to improve reliability and Cu filling margins. In recent years, the application of this technology has been expanding, with plans to deploy it in DRAM processes. We have reported previously on our CVD-Co equipment and deposition technology[5]. In this paper, we introduce the film properties (thickness, resistance, and step coverage) required for Co liners and the results of our filling evaluation.

1) Thickness and resistance

The Co film layer used in a Co liner requires a thickness of 1 to 2 nm. Fig. 8 shows how resistivity and surface morphology depend on the film thickness.

The lower the film thickness, the higher the resistivity. By optimizing the deposition conditions at a film thickness of 1.5 nm, we obtained a Co film with a resistivity of about 10,000 μΩcm. In addition, the morphology indicates a dense film profile with low roughness.

2) Step coverage characteristics

Fig. 9 shows TEM images of the Co coverage evaluation results using a patterned substrate (trench width 17 nm, AR 4.3). A Co film having a thickness of 2 nm was uniformly formed on the trench wall, indicating good step coverage results.

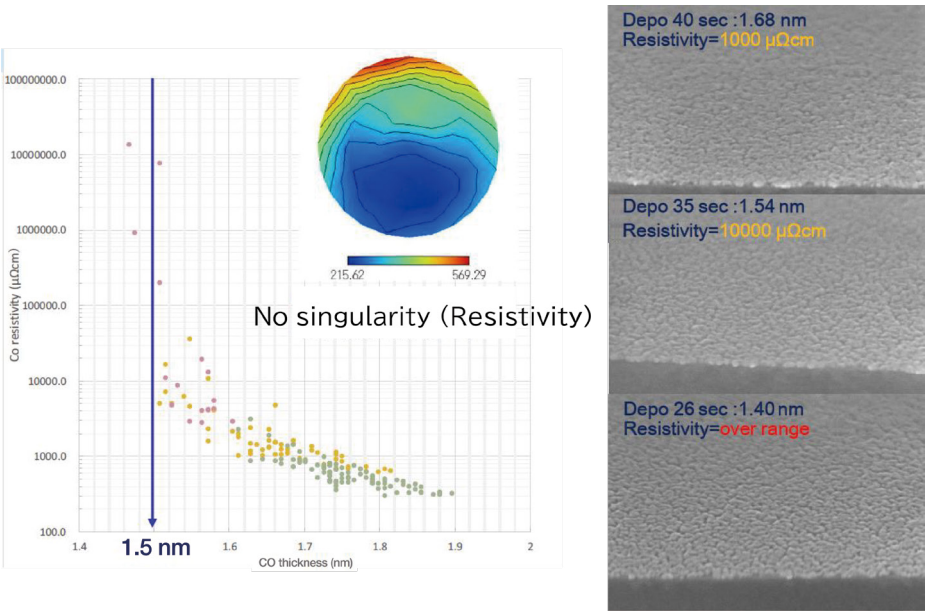


Fig. 8 Co film resistance and surface SEM

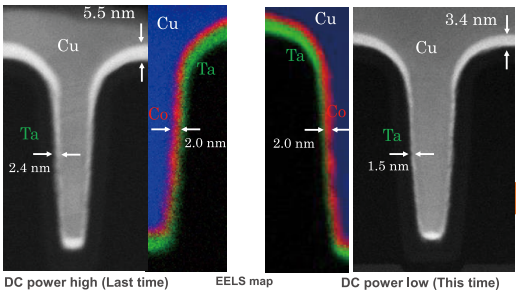


Fig. 9 Co Coverage

3) Cu reflow filling

Fig. 10 shows the Cu reflow process used to evaluate the filling of Cu into 300 mm diameter wafers. Fig. 11 shows cross-sectional views of the patterned substrate at the center of the wafer and at a position 3 mm from the wafer edge. We confirmed that close to 100% filling into the wafer surface was achieved. We also evaluated filling into pattern profiles with A/R values of 2 to 10 at a trench depth of 220 nm. Fig. 12 shows that good Cu filling is possible in all of the pattern profiles.

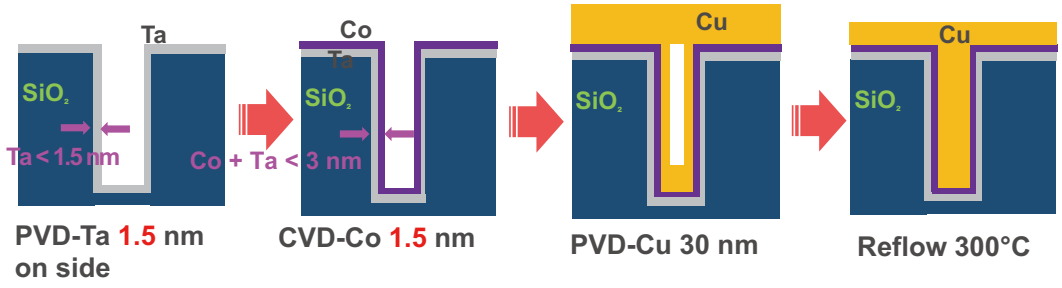


Fig. 10 CVD-Co reflow process

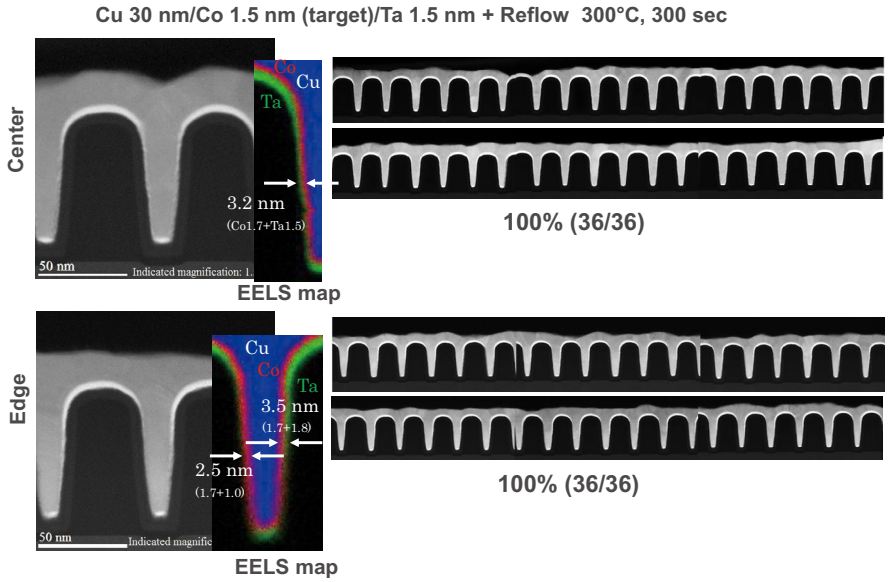


Fig. 11 TEM observation after reflow

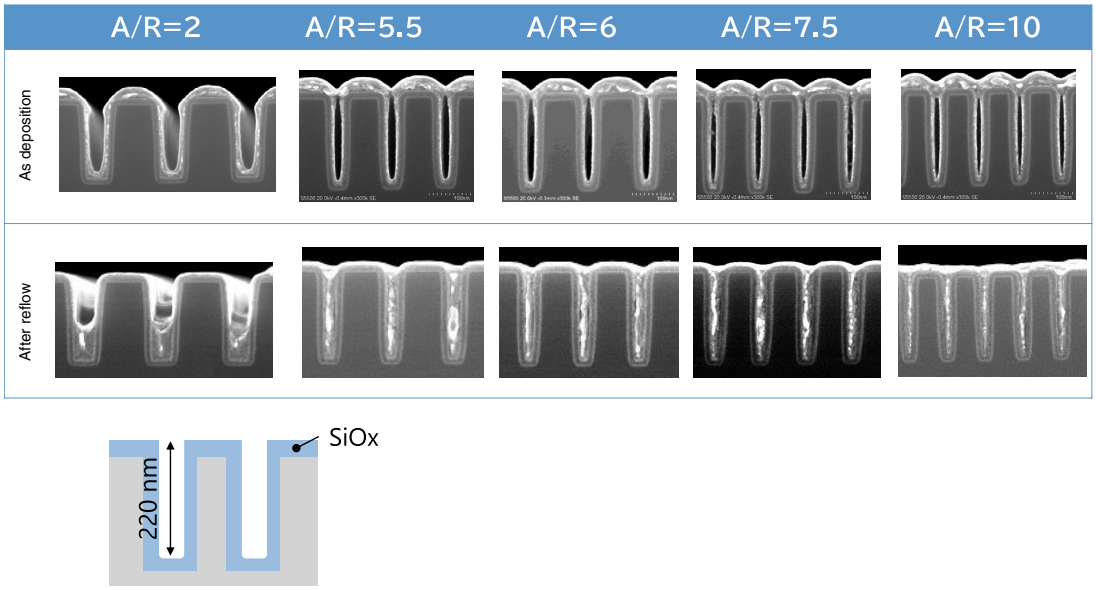


Fig. 12 Cu reflow margin

5. Summary

We have developed several Cu interconnect technologies for semiconductor devices, including remote plasma, Cu sputter, and CVD-Co technologies. These technologies are expected to be applicable to memory devices such as DRAM, as well as logic devices. Going forward, we expect that Cu interconnect technologies for semiconductor devices will continue to be required to support further miniaturization. As equipment manufacturers, we need to accelerate the development of equipment that meets market demands and endeavor to supply equipment with high added value.

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